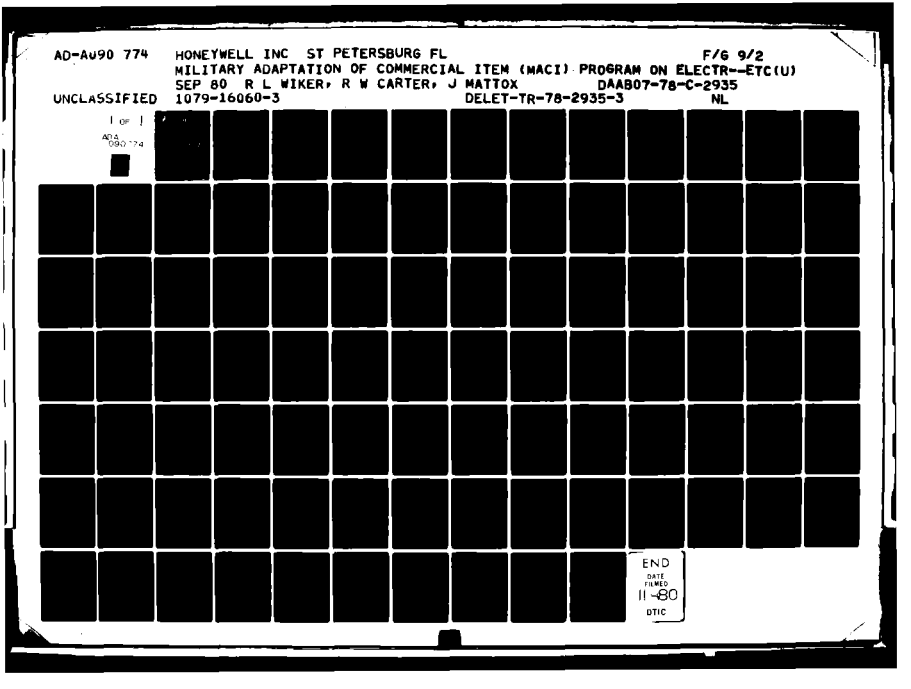
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Research and Development Technical Report
DELET-TR-78-2935-3

MILITARY ADAPTATION OF COMMERCIAL ITEM (MACI) PROGRAM ON ELECTRICALLY ALTERABLE READ ONLY MEMORY

Richard L. Wiker

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September 1980

Third Interim Report, for period 15 December 1979 — 15 May 1980

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The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

The attached report is based on limited sample tests performed to date. All tests to be performed are not complete. In addition, it must be recognized that tests were performed to the specifications in MIL-STD-883-B and may be more restrictive than the respective vendor's data sheet.

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20 ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Development of Accelerated Testing of Unique MNOS Characteristics.

Metal Nitride Oxide Semiconductors

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FIGURES

FIGURES

1. INTRODUCTION

The objectives of the MACI-EAROM Program were previously stated in the First and Second Interim Reports. Due to the unusual nature of the EAROM/WAROM devices under study in this program, the job of developing a useful and practical slash sheet and test plan is uniquely complex and difficult. This is particularly true due to the fact that those manufacturers that supply the devices either are not eager to sell to a military market or are in the early stages of specifying and characterizing for that range of operation.

While all the normal complexities of memory device evaluation still apply to EAROM/WAROM devices, additional dimensions of time retention data and the variation of that parameter and others as a function of number of write/erase cycles compounds the specifying and testing problems. Other effects like read, disturb, retention and temperature effects on writing, erasing and endurance required a potential user to have an in-depth understanding of the MNOS technology to properly apply these devices to his systems.

In most cases, accelerated tests for monitoring these complex parameters have either not been developed or are not widely known or published. The specifying of these test parameters is even more difficult due to a lack of a broad data base of characterization data.

This program pioneered in several of these uncertain areas of parameter testing and prediction due to the glaring need to provide some kind of definition and organization to those seeking a cost effective solution to alterable non-volatile memories. The baseline for tests that predict which devices will "wear-out" faster and be disturbed sooner by read cycling was developed and some correlation to expected results shown. The significance of these tests to potential user cannot be overestimated.

Previous methods for determining endurance and read disturb effects were limited to lot sampling tests which either destroyed the parts or took long periods of tests to measure and showed very poor correlation to the actual performance of the remaining parts in the lot. Due to this uncertainty in sorting out poor performing parts prior to systems application, many potential users were diverted to other less cost effective solutions. By allowing 100 percent testing of MNOS parts, direct indication of each device's potential performance reduces the risk of experiencing in situ failures in critical field situations. While the empirical data base established is still small, relative capabilities of parts can be established which allows sorting by critical parameters, minimizing the probability of system level failures which is significantly better than previous methods. Section 8 covers the progress in this important area.

The First Interim Report (DELET-TR-78-2935-1) covered the Pre-selection Phase of the contract which developed the selection criteria for picking which devices would be considered as candidates for selection as the most suitable devices for military applications. These criteria were developed from surveying potential users from military, government and defense contractor areas to determine desirable device organizations and performance parameters.

The results were used to select five device types and to establish the characterization tests to be performed. Once the devices were selected, each potential manufacturer was surveyed and questioned on quality control and inspection procedures and these compared to MIL-STD-883-B specifications. The performance of each type device was characterized for speed, power, radiation resistance, retention, endurance, read disturb effects and DC parameters and the results presented. Endurance prediction techniques were developed and correlated to endurance measurements taken. Package testing, including lead pull, temperature cycling and shock, fine and gross leak and vibration were performed on all devices. In addition the first report covered potential applications and chip photomicrographs.

The second Interim Report (DELET-TR-78-2935-2) clarified some of the results shown in the earlier report and further reported on the writing characteristics and total dose radiation performance. It presented the comparative performance data in matrix form and detailed the reason for selection of the NCR 2451/ER3400 as the candidate part for potential military qualification. DC parameter data such as input/output levels, power performance and leakage current were examined. A preliminary form of a final test plan was shown for the selected parts.

This report picks up from where the last report finished and details the last phase of the MACI program which is concluded by the delivery of 50 fully-screened parts, a proposed slash sheet and the Final Test Plan.

2. SCOPE

This report covers the following areas:

- Provide background for evaluation of data presented
- Update information on MNOS device status
- Discusses results of screen and performance testing

- Discusses trends of performance analyzed from screen and performance testing
- Presents the proposed slash sheet for ER3400/NCR2451 devices
- Presents the final version of the test plan
- Discusses accelerated test methods for endurance, read disturb and retention
- Demonstrates a monograph developed for accelerated retention measurement and prediction
- Conclusions drawn from results of testing and vendor interface.

3. PROGRAM PLAN

The program plan shown in Figure 2-1 shows the progression of the MACI program. The shaded area to the right of this diagram shows the portion completed in the third phase of the MACI program. The remaining deliverables are left to be discussed and analyzed on the final report.

4. BACKGROUND

The two previous MACI EAROM reports covered the pre-selection phase, the selection of a final device type, some performance data and the development of the Test plan for screening the devices. The last report paid particular attention to the writing characteristics of these devices. It showed the relationship between write, voltage levels and written threshold level. In addition, the relationship between write time and threshold was explored. Another area investigated was the effect of Total Dose Radiation levels on the data thresholds and read access times of the MNOS memory devices.

The MACI program attempts to provide some definition to areas of the MNOS technology not formally defined at this time, by industry standards. As a result, some approaches shown in this report may be at variance with the ultimate standard that is set in some parameters. Due to the complex nature of the interrelationships between the time related parameters (i.e., retention, read disturb, endurance), it is necessary that a potential user have a full understanding of the technology before applying it in his systems. The MACI results can therefore be used as a base upon which a more thorough understanding can be built.

Due to the limited nature of the MACI program, it should be known by potential users of the results presented that the data base from which they are drawn is very narrow. In each case, the testing was

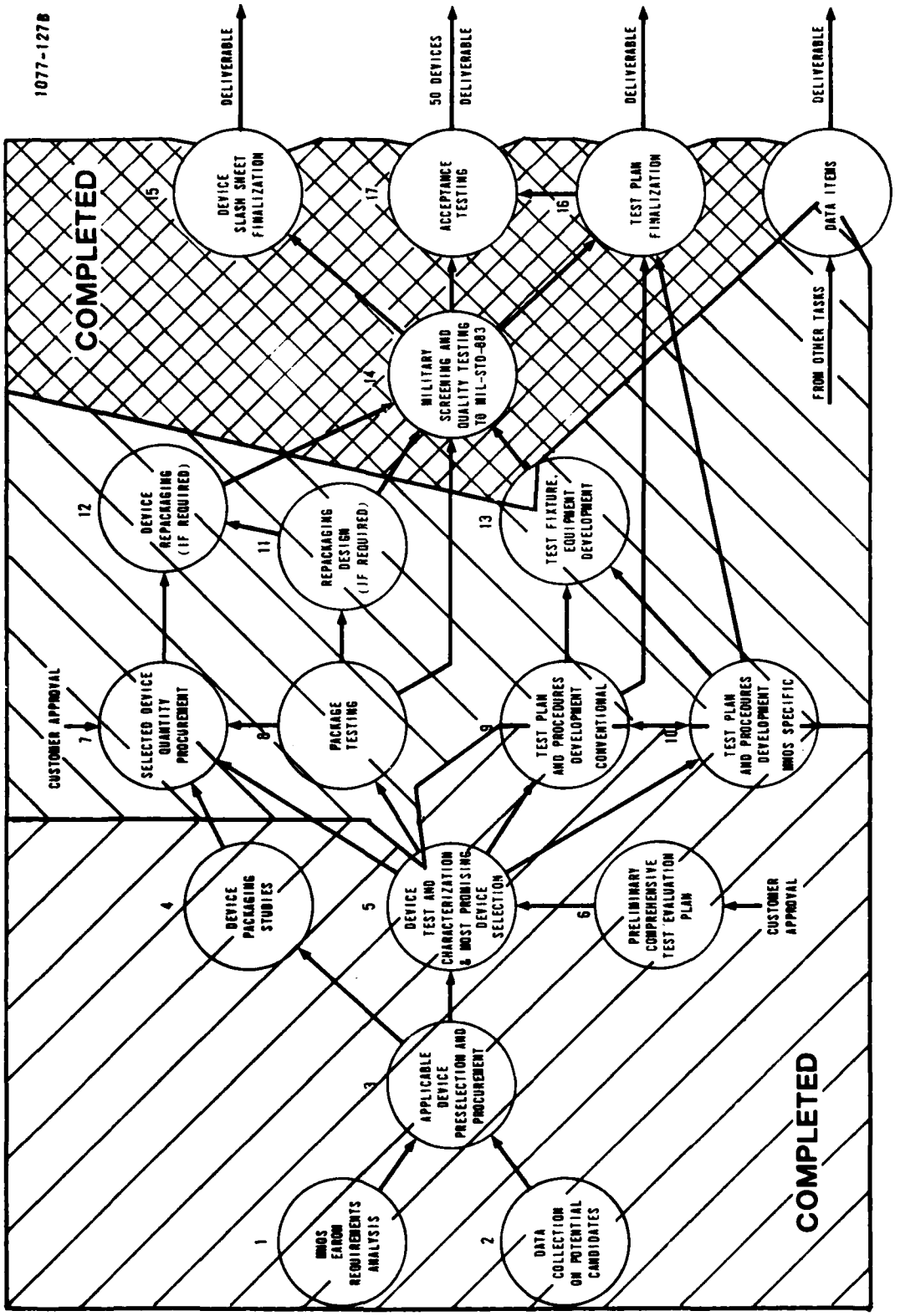

FIGURE 2-1. MACI-MNOS EAROM PROGRAM

performed on either a single lot or across a few lots and the results may be more indicative of that lot than the general run of similar devices produced. It is recommended that anyone wanting to use the results shown perform similar characterizations themselves to confirm the relationship shown in this report.

The relationships used to create the accelerated or predictive tests are well known and established. Empirical data indicated that, assuming similar nitride quality and oxide thickness, the endurance of MNOS devices was directly related to the relative thickness of the nitride layer in the gate region. It is also well established that nitride thickness bears an inverse relationship to the speed with which a device can be erased. By combining these two relationships, a test was developed using a "soft" erase following a full write to indicate which devices had thicker nitride layers and thus would exhibit longer endurance. With all devices subjected to these measurements, devices selected to be at opposite ends of the spectrum of nitride thicknesses were tested for endurance to determine if a correlation could be established. When the results were encouraging, further study was indicated. The impact of endurance prediction is significant if it can eliminate most low endurance parts from reaching systems in the field. While this method is currently relatively crude and with little supporting data base, it appears far superior to lot sampling endurance testing in correlation to devices being screened.

5. MEMORY DEVICE STATUS

The availability status of several of the original candidate devices has undergone change since the second MACI report.

- The Nitron NC7810 is now available but is limited to +85 degrees C operation due to a relatively low retention at high temperature. Work is being performed to improve and extend the range of this part.

- General Instruments is making both military grade 2810's (ER2810 HR) and industrial grade parts (ER2810 IR).

- General Instruments is now making ER2810's in leadless carriers called ER2810 LP.

- NCR has now adopted a policy of being more open to OEM sales, making the parts they previously sold available now for commercial sale.

- The Hitachi 16K N-channel MNOS EEPROM is now available in sample quantities. It is pin compatible with versions of the 2716 UVEPROM, has a single 5V supply and boasts a 300 ns max access time.

- General Instruments will introduce a 1K N-channel EAROM approximately at the beginning of 1981 with an access time of 300 ns organized 128 wds bu 8 bits, and plans to introduce a 16K Bit P-channel part at approximately the same time.

- LPCVD Nitride parts being shipped from GI show similar characteristics to the older reactor parts with some indication that a lower yield to +125 degree C retention requirements may result. Some effects on read disturb and endurance characteristics appear to be resulting also. Contact GI for details.

- Nitron is not yet selling the NC7451 parts due to some initial start-up problems with developing the part.

- Military interest in MNOS memories is rising, particularly with regard to radiation hardened applications to replace expensive power consuming magnetic alternatives.

These sources of common parts remain as viable sources for MNOS devices with new Japanese related parts becoming available as single sourced parts. The switch to N-channel parts should accelerate demand for this technology in the near future.

6. FINAL TEST PLAN

The final test plan is shown below. Modifications to the burn-in circuit and addition of a voltage reference test were the main changes from that shown in Interim Report Number Two.

980-16962

FINAL TEST PLAN

MILITARY ADAPTATION OF A COMMERCIAL ITEM

(MACI)

PROGRAM ON MNOS EAROM(WAROM)

Prepared by:_____
R.W. Carter
Component Application

Approved by:_____
R. Wiker
Technical Director

1.0 INTRODUCTION

This final test plan details the test methods and procedures to be used for 100 percent preconditioning, screening and lot quality conformance inspection of commercial MNOS WAROM devices for use in military applications.

The sequence of tests and procedures will be as follows:

A. Device Procurement

B. 100 percent Preconditioning and Screening

C. Lot Quality Conformance Inspection

D. Deliver 50 units

E. Deliver Slash Sheet

F. Deliver Final Report

1.1 Device Type

The device type that was determined to be the most suitable for military applications in the MACI preselection phase is the 3400/2451 1024 x 4 bit Word Alterable Read Only Memory (WAROM).

2.0 GENERAL

2.1 Applicable Documents

The following documents of the issue in effect on the date of this test plan, apply to the extent used herein.

MIL-M-38510 Microcircuits, General Specification for

MIL-STD-883 Test Methods and Procedure for Microelectronics

2.2 Electrical Tests

2.2.1 DC Parametric Tests

DC Parametric tests will be as specified in Appendix A.

2.2.2 AC and Functional Tests

AC and Functional Tests will be as specified in Appendix B.

2.3 Device Procurement

255 devices total will be procured: 225 - from General Instrument (G.I.), and thirty from National Cash Register (NCR).

3.0 PROCEDURE

Devices will be processed according to the Final Test Plan shown in Figure 3.0.

3.1 100 Percent Preconditioning and Screening

Preconditioning and Screening will be in accordance with method 5004 of MIL-STD-883 Level B and Table 3.1 herein and will be conducted on all devices prior to lot quality conformance inspection. The following conditional Criteria will apply:

a. Burn-in Test - Burn-in circuit of Figure 3.1a will be used.

b. Interim and Final Electrical Tests - Interim electrical tests will consist of the tests specified in Appendix B-1 and B-2 at an ambient of +25°C. After a one hour soak at +125°C, the test specified in Appendix B-3 will be conducted and the resulting V_T values and time recorded.

   Following Burn-in, Final electrical tests will consist of the tests in Appendix B. The initial test will be that specified in B-3 at +25°C with the threshold and time recorded. The remaining tests will be performed at -55°C, +25°C and +125°C ambient using the tests specified in Appendix A and B-1. After Burn-in V_{REF} is measured and recorded on each device via test specified in B-4.

3.2 Quality Conformance Inspection

From the devices which have successfully passed the 100 percent Class B screening, 119 samples will be submitted to the Quality Conformance Inspection requirements specified in Method 5005 of MIL-STD-883. This inspection will be composed of Group B and C tests. Group D (package related) tests were performed in the preselection phase and are not necessary to repeat. The tests and sample sizes for each group are summarized in Tables 3.2.1 and 3.2.2.

3.2.1 Group B Inspection

Group B inspection will be in accordance with Table 3.2.1 herein and as follows:

A. Subgroups 1 and 6: Physical dimensions and internal water vapor content were performed in Group D inspection and are not necessary to repeat here.

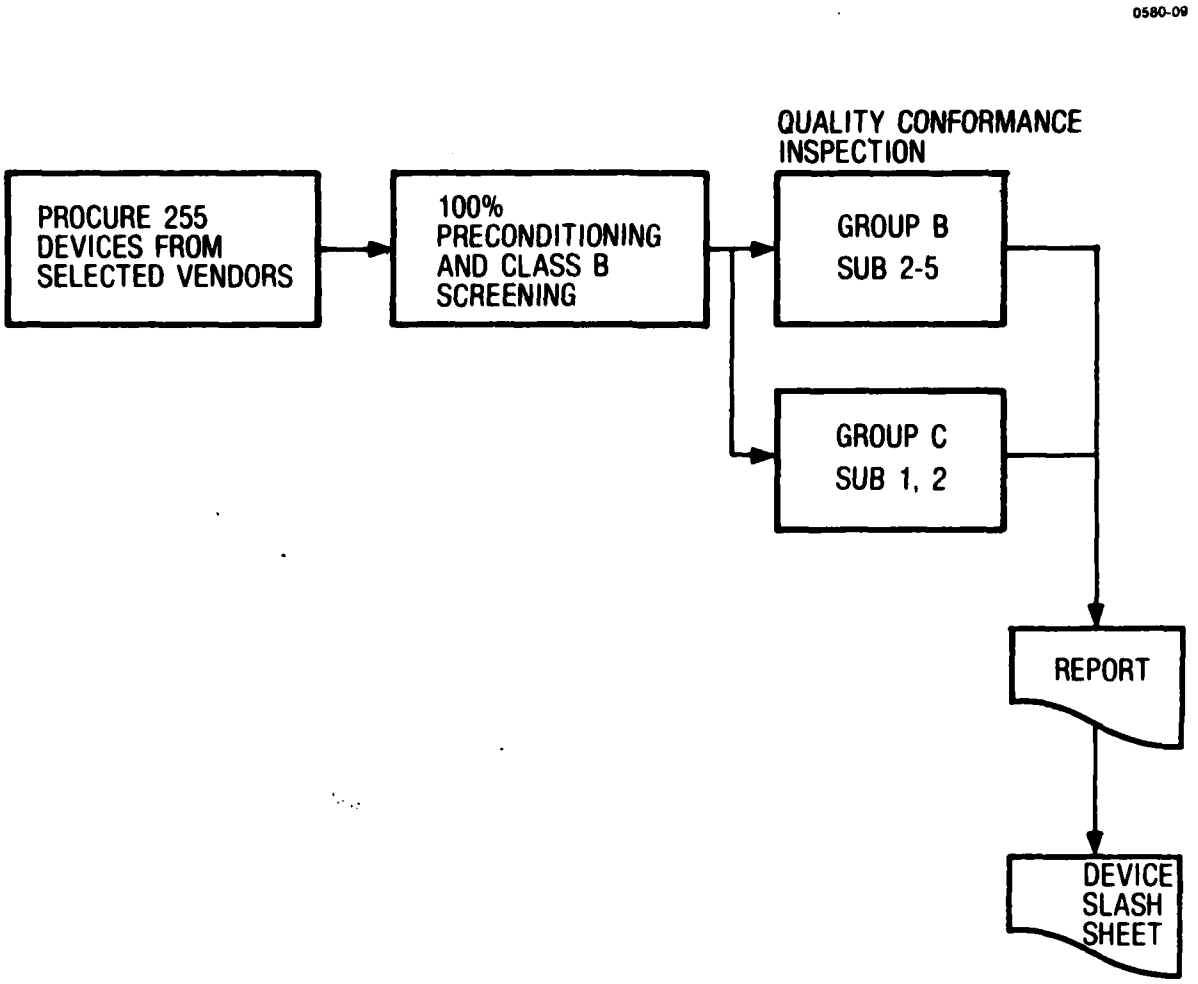

FIGURE 3-0. FINAL TEST PLAN

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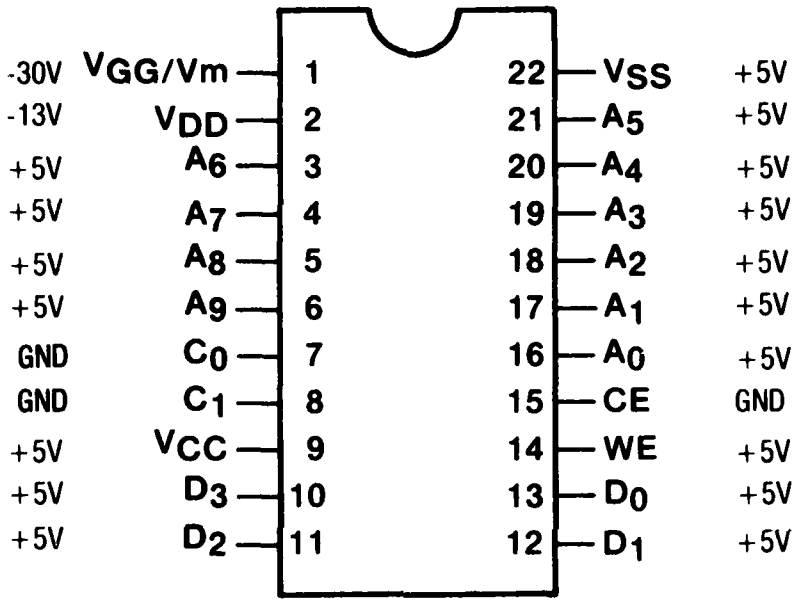

FIGURE 3-1a. BURN-IN CIRCUIT

TABLE 3.1. 100 PERCENT PRECONDITIONING AND CLASS B SCREENING TESTS

Examination of Test	MIL-STD	Method Number	Details
Stabilization Bake, No end point measurements required	883	1008.1	24 hours Condition C *1
Temperature Cycling	883	1010.2	Condition C *2
Constant Acceleration	883	2001	Condition E Y_1 only
Seal Fine Gross Serialization Soak @ +125°C	883	2020	Condition A or B
Pre-Burn-In Electrical Test Functional Tests AC Tests		See 3.1b	
Burn-In Test	883	1015 See Fig. 3.1a	Condition C 168 hours at 125°C
Final Electrical Test DC Parametrics Functional Test AC Test		See 3.1b	
External Visual	883	2009	

TABLE 3.2.1. GROUP B TESTS 1/

Test	MIL-STD-883 Method	Condition	LTPD	Sample Size ACC#=0
Subgroup 1				
Physical dimensions 2/	2016		2 devices (no failures)	2
Subgroup 2				
Resistance to solvents	2015		3 devices (no failures)	3
Subgroup 3				
Solderability	2003	Soldering temperature of 260 ±10°C	15	3
Subgroup 4				
Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document.	1 device (no failures)	1
Subgroup 5				
Bond strength Thermocompression	2011	Test conditon C or D	15	10

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.

2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.

TABLE 3.2.2. GROUP C (DIE-RELATED TESTS)

Test	MIL-STD-883 Method	Condition	LTPD	Sample Size	Accept No.
Subgroup 1					
Steady state life test	1005	Test condition to be specified (1,000 hours at 125°C)	5	77	1
Subgroup 2					
Temperature cycling	1010	Test condition C	15	25	1
Constant acceleration	2001	Test conditon D Y_1 orientation only			
Seal					
(a) Fine					
(b) Gross					
Visual examination	1010 or				
End-point electrical parameters	1011				

B. All devices selected for testing will be programmed with an asymmetric slant pattern. After completion of all testing, the devices will be verified and erased (except those devices submitted for Group C testing.

3.2.2 Group C Inspection

Group C inspection will be in accordance with Table 3.2.2 herein and as follows:

A. End point electrical parameters - End point electrical parameters will be as specified in Appendix B at ambient temperatures of -55°Cm +25°C abd +125°C.

B. Steady State Life Test - Steady State life test will be performed using the circuit of Figure 3.1a.

3.3 Deliverable Devices

Of the remaining devices which have passed Group C inspection (and therefore screening), fifty devices will be selected as deliverable devices.

3.4 Final Report and Slash Sheet

The screening and lot acceptance test results will be presented in a summary report. A MIL-M-38510 type slash sheet will then be developed from this test data.

7. SCREEN TEST AND PERFORMANCE

Test Results.
Using the Final Test Plan shown in Section 6.0, the ER3400/ NCR2451 devices bought for the MACI program were tested.

7.1 Yield. Out of 160 devices screened, using the test plan, 50 devices passed all tests for a yield of 31.25%. Figure 7-1 illustes where the yield loss occurred (what tests). Ninety-six devices were held for destructive tests (i.e., endurance, lead pull, etc.).

7.1.1 Leak Test. Out of 160 devices placed in preconditioning tests including:

o Stabilization Bake	Method *1008.1 Cond. C
o Temperature Cycling	Method 1010.2 Cond. C
o Constant Acceleration	Method 2001 Cond. E only
o Seal - Fine	Method 2020 Cond. A or B
Gross	
Serialization Soak	
@ +125 deg C	

140 devices passed with most failures in fine leak.

*MIL-STD-883

7.1.2 Pre-Burn-In Electrical Test (Screen Tests).

(Section 3.1b Test Plan)
As can be seen from Figure 7-1, 30 devices out of 140 failed these tests. Most failures were NCR2451 failing at -55 degree C with a few ER3400's failing at +125 degree C.

7.1.3 Post 160 Burn-In Retention Tests. The primary cause of yield loss of ER3400 devices resulted from poor retention at +125 degree C. Using a criteria of 1 year of retention at +125 deg C and plotting the minimum "0" threshold after 1 hour at +125 degree C and after 160 hours at +125 deg C on a lin-log graph of threshold against the log of time from write, the intersection of the voltage reference value minus the operating offset can be extrapolated. From this point, the retention time can be determined from the time scale. If this point exceeds 1 year, the device is considered an acceptable part.

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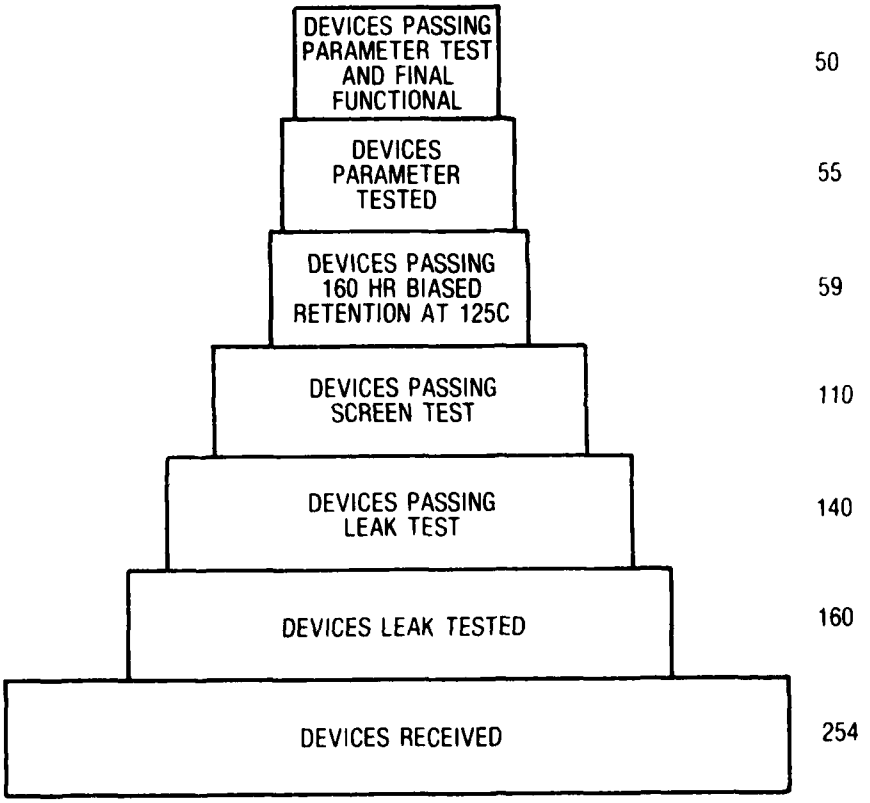


FIGURE 7-1. YIELD LOSSES

There appeared to be a significant change in the high temperature retention characteristics of ER3400 parts bought in February of 1978 and February 1979. The earlier parts exhibited a smaller change in retention slope (VT/Time) from +25 deg C to +125 deg C than the newer parts and thus had better retention at the higher temperature. Graph 7-1 shows that only 59 devices out of 110 devices tested for high temperature retention passed the 1 year requirements. Only a few of the NCR2451's failed this test with the vast majority of failures being ER3400's.

Figure 7-2 is a plot of a typical ER3400 (per #811) showing the screen test retention measurement. The significant change in retention slope from the +25 degree C section of the plot to the +125 degree C section can be seen (i.e., from 0.4V/decade to 1.3V/decade). Figure 7-3 shows a plot of a typical NCR2451 (also typical of earlier ER3400's). This plot shows that the change in slope from the +25 degree C section of the curve to the +125 degree C section as slight (i.e., from 0.55v/decade to 0.58V/decade). While the yield on the earlier ER3400's was estimated at approximately 70 percent to this parameter, the yield of the newer parts appears more like 50 percent.

A second Burn-In Period was held for several of the newer ER3400's. The results showed that approximately 46 percent of the devices that showed poor retention slopes during the first burn-in period recovered after the second burn-in to produce an acceptable retention at high temperature.

Figure 7-4a shows the distrubution by Post Burn-In retention slope of all parts initially tested. The significant difference in the Post Burn-In slope of the ER3400's from the NCR2451's. Figure 7-4b shows the final distribution of Post Burn-In slopes for all parts tested. A noticeable shift in ER3400 retention slopes can be seen.

This suggests that perhaps other effects besides simple discharge of the memories is the cause of the initial change. Some indication of a possible permanent threshold shift at high temperature soak taking place is suggested. The second burn-in cycle is then taken to be mostly discharge since it appears that all initial permanent threshold change has been baked out.

Illustrating the point regarding the "annealing effect" of the +125 degree C soak some of the ER3400's were placed in second and third 160 hour burn-in periods with retention measurements taken according to the normal screening method. Figure 7-5 shows an ER3400 which after three burn-in periods still fails a 1 year retention criteria at +125 degree C. However, Figure 7-6 illustrates one of

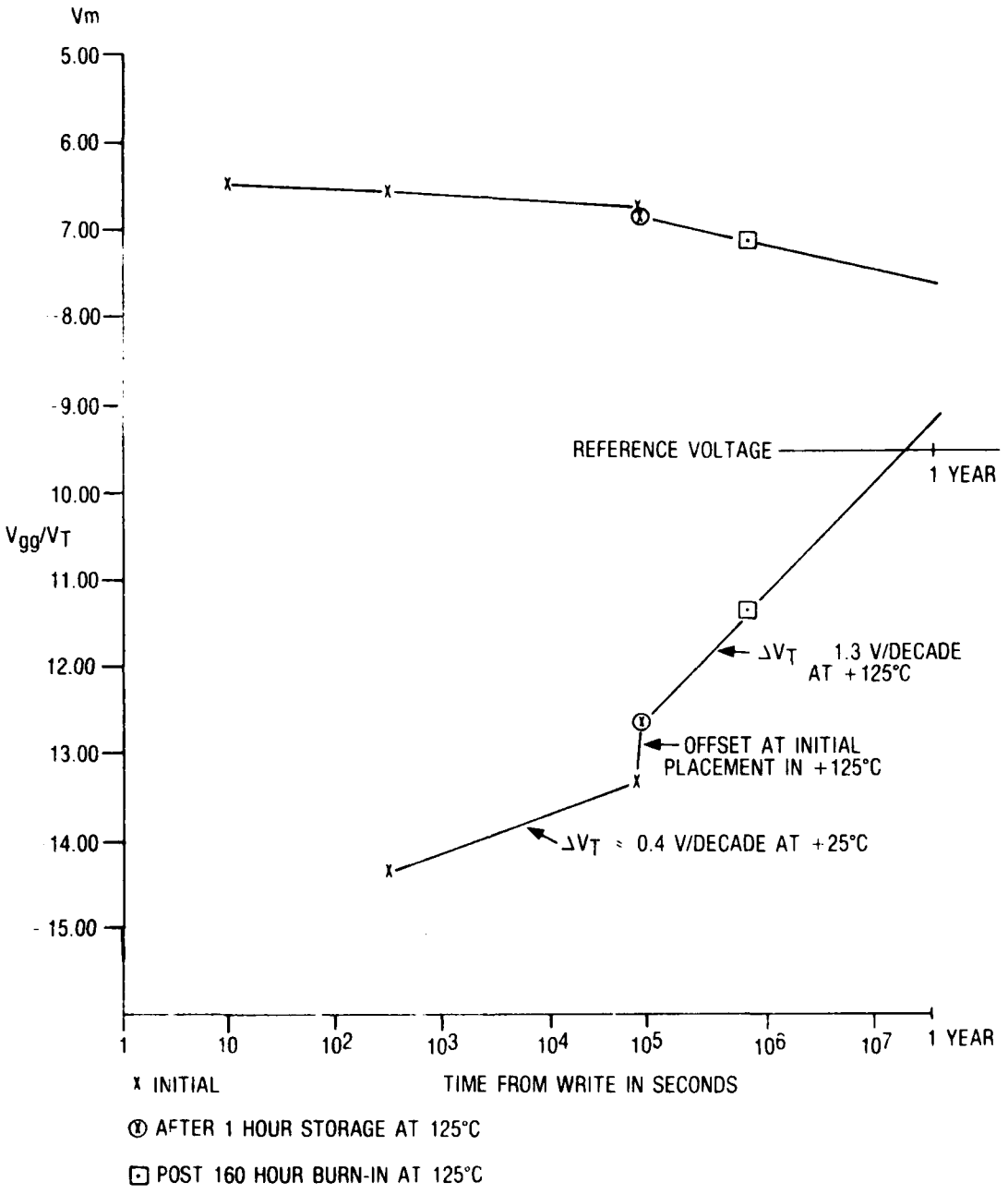


FIGURE 7-2. HIGH TEMPERATURE RETENTION TEST FOR ER3400

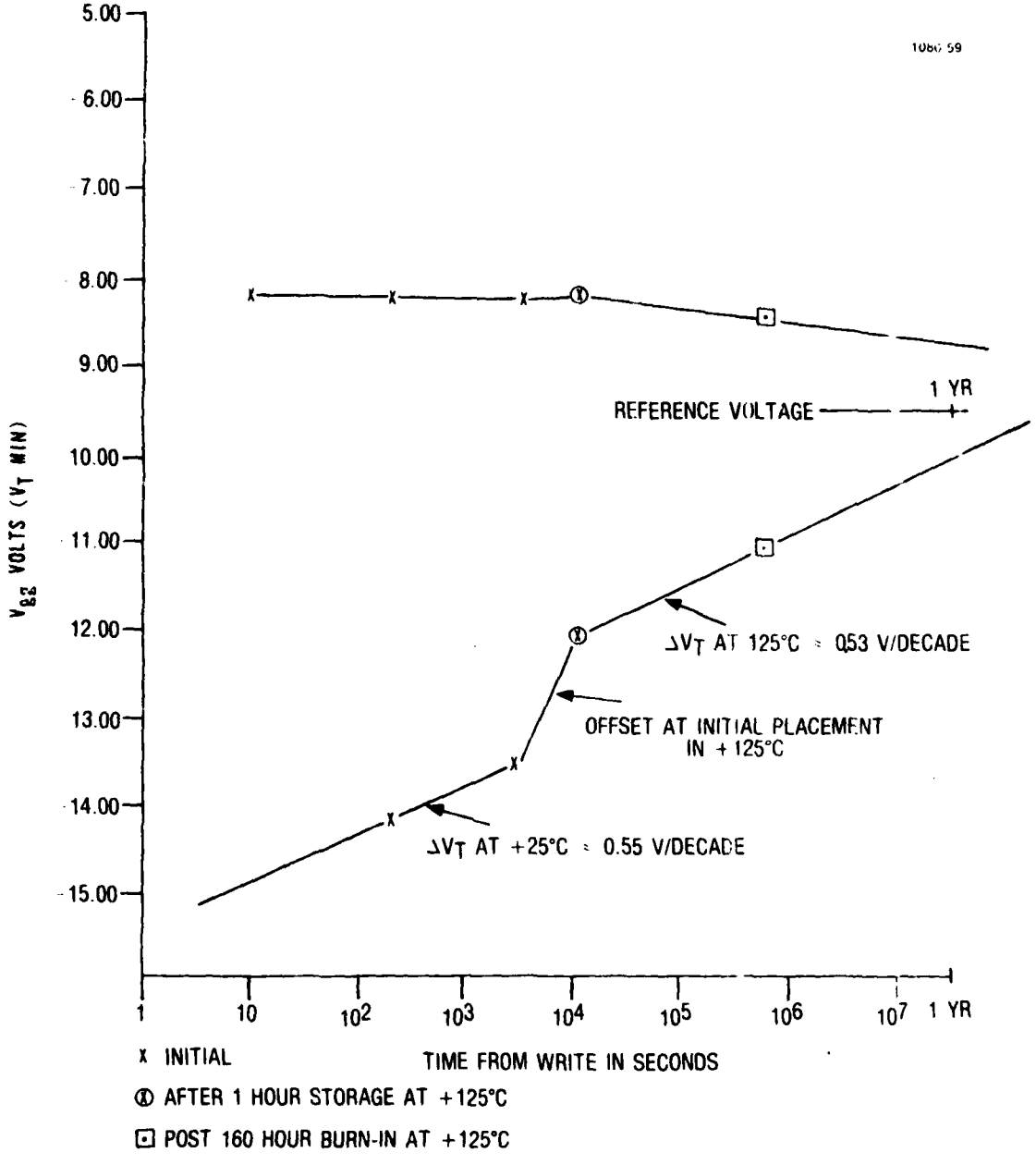


FIGURE 7-3. HIGH TEMPERATURE RETENTION TEST FOR NCR2451

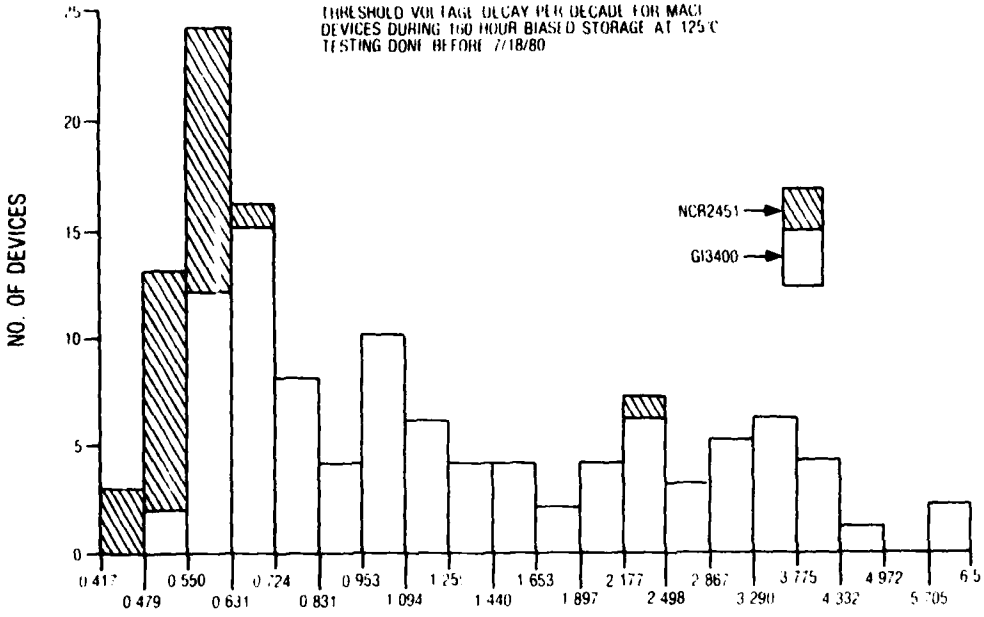


FIGURE 7-4 b. FINAL POST BURN-IN RETENTION SLOPE

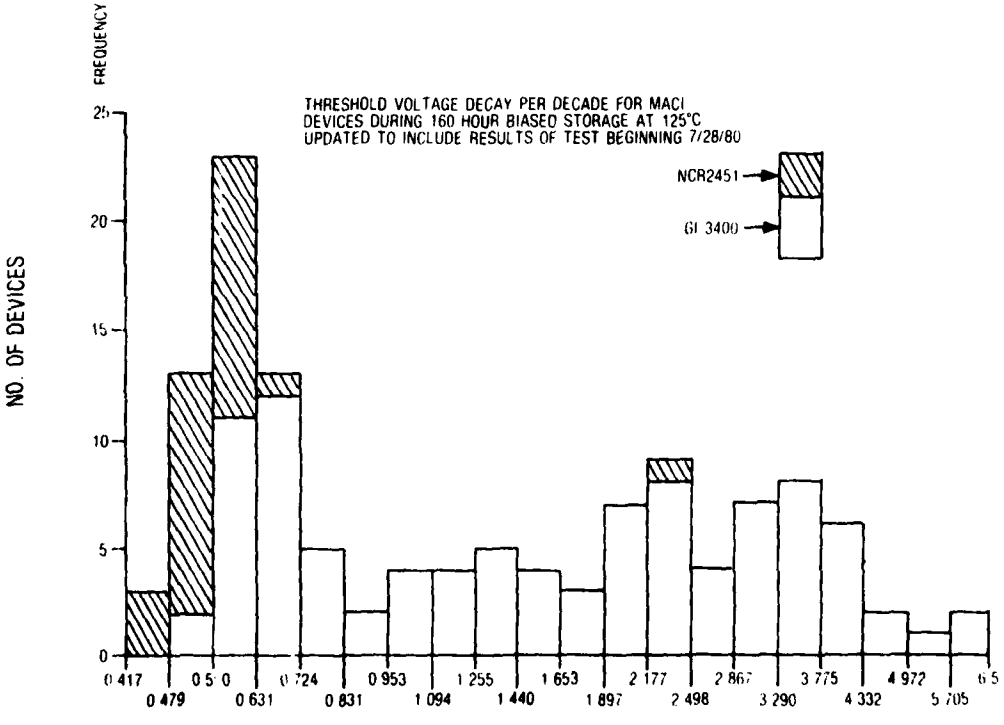


FIGURE 7-4 a. INITIAL POST BURN-IN RETENTION SLOPE

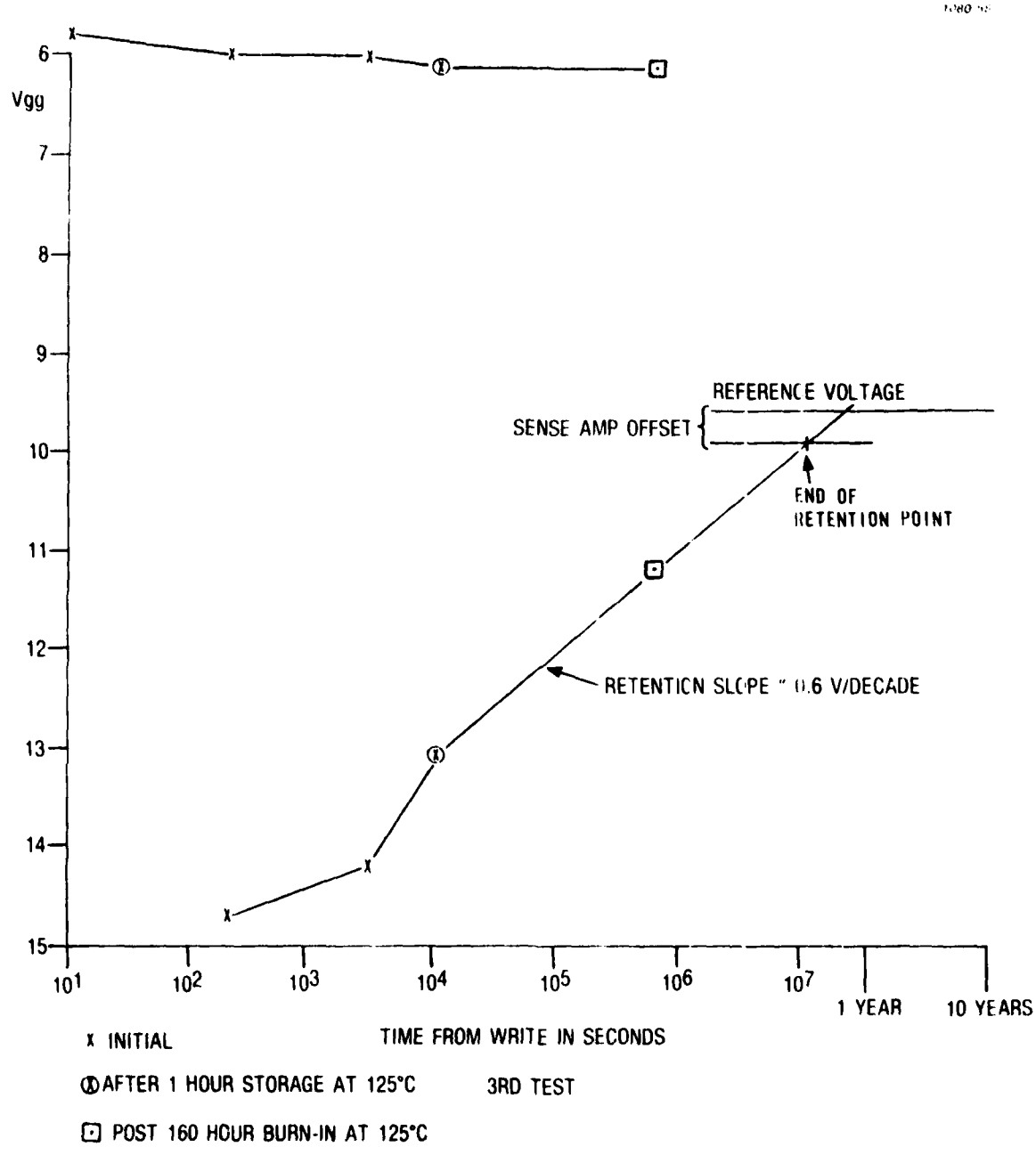


FIGURE 7-5. THIRD BURN-IN FOR ER3400 DEVICE NO. 863

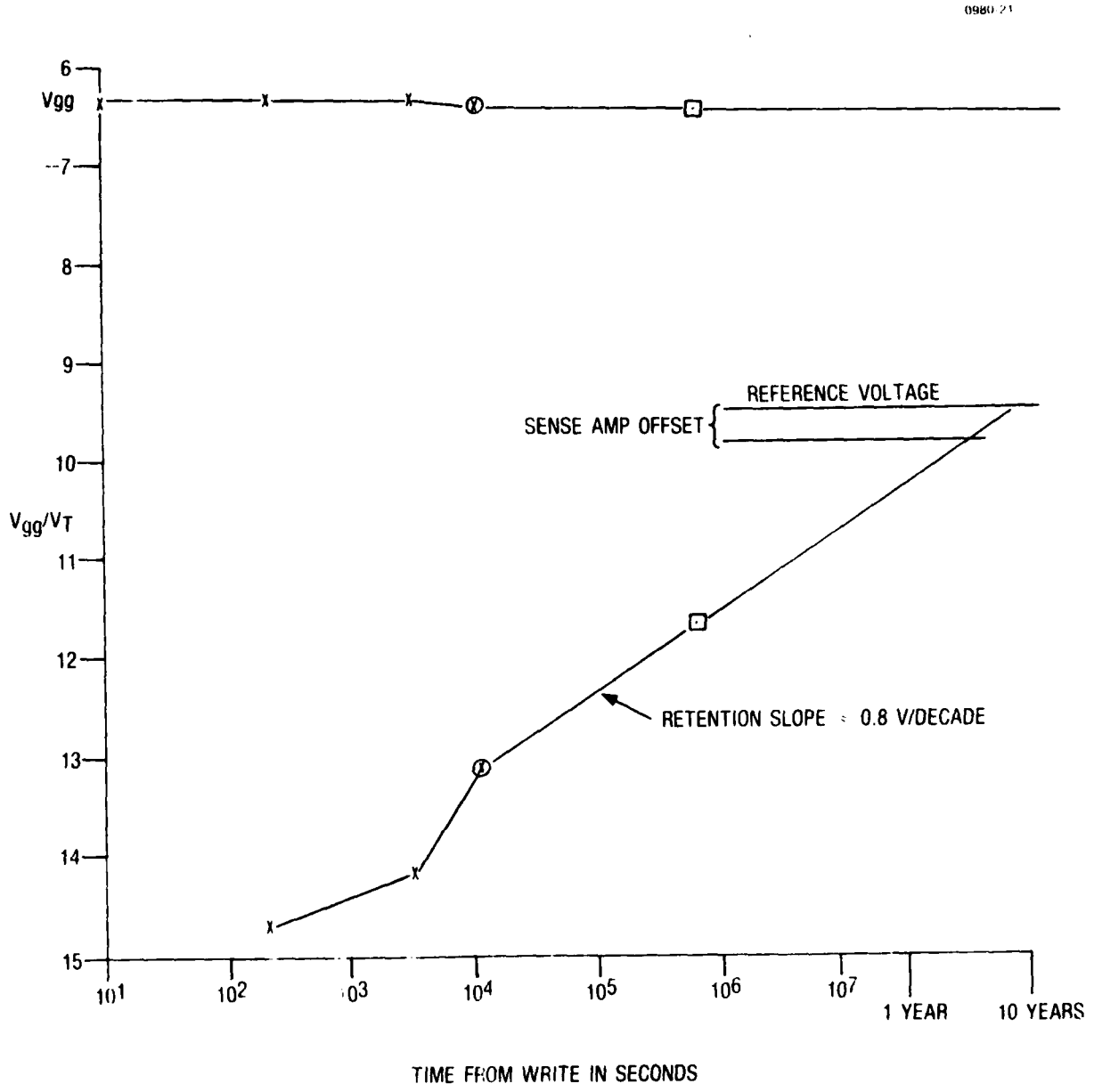


FIGURE 7-6. SECOND BURN-IN PERIOD FOR ER3400 DEVICE NO. 832

the ER3400's which initially failed retention after burn-in at +125 degree C. After a second burn-in period of 160 hours at +125 degree C, this device now exhibits a predicted retention of 3 years at +125 degree C. Figure 7-7 shows the extreme case where device #875, which would not pass 1 year retention at +125 degree C after the first burn-in, was estimated to have 225 years retention at +125 degree C after the second burn-in period.

In an attempt to gauge if the change from Reactor Nitride to the LPCVD process was the significant factor in the Retention Slide, several ER2810 parts made with the newer LPSVD process were tested for retention. Figures 7-8 and 7-9 show the results of that study. The indication is that since the ER2810 parts performed well at +125 degree C that the problem exists in the ER3400 design or process. Since the earlier parts did not exhibit the problem, some other or combination of changes appears to be the underlying cause. This does not rule out LPCVD process effects being more significant to the one transistor/cell ER3400 than the transistor plus reference row type design of the ER2810.

Figures 7-2, 7-3, and 7-4 point out a "Sense Amp Offset" value of 0.35V with respect to the internal "Reference Voltage". Both of these parameters have significant effect on the retention prediction in the ER3400/NCR2451 type devices. The Reference Voltage refers to an ihternally generated voltage used to compare against the threshold voltage of the memory transistors. The value of this Reference Voltage can be measured externally by methods described in the test plan.

Figure 7-10 shows the distribution of Internally Generated Reference Voltages of all ER3400/NCR2451 parts tested in the MACI program. The maximum measured value was -10.24 volts while the minimum was -9.02 volts with the mean value being -9.55 volts. Figure 7-11 shows the same distribution for parts passing the screen tests.

While the sense amp compares this value against the memory transistor threshold allowance must be made for the sensitivity of the sense amp itself.

An empirical way of testing for this sensitivity was devised. By "soft" erasing "zeros" until they failed normal read cycling and then measuring the threshold, a typical offset value could be determined. Figure 7-12 shows the distribution of the measured sense amp offset values for all MACI ER3400/NCR2451 parts. Figure 7-13 shows the sense amp offset values for the parts passing all the screening tests and shipped to ERADCOM. As can be seen from the plots in both figures, if a value of 0.35V is adopted as "standard" offset number, more than 90 percent of all parts fall at or below that value causing estimated retention values to be conservative and accurate. By using

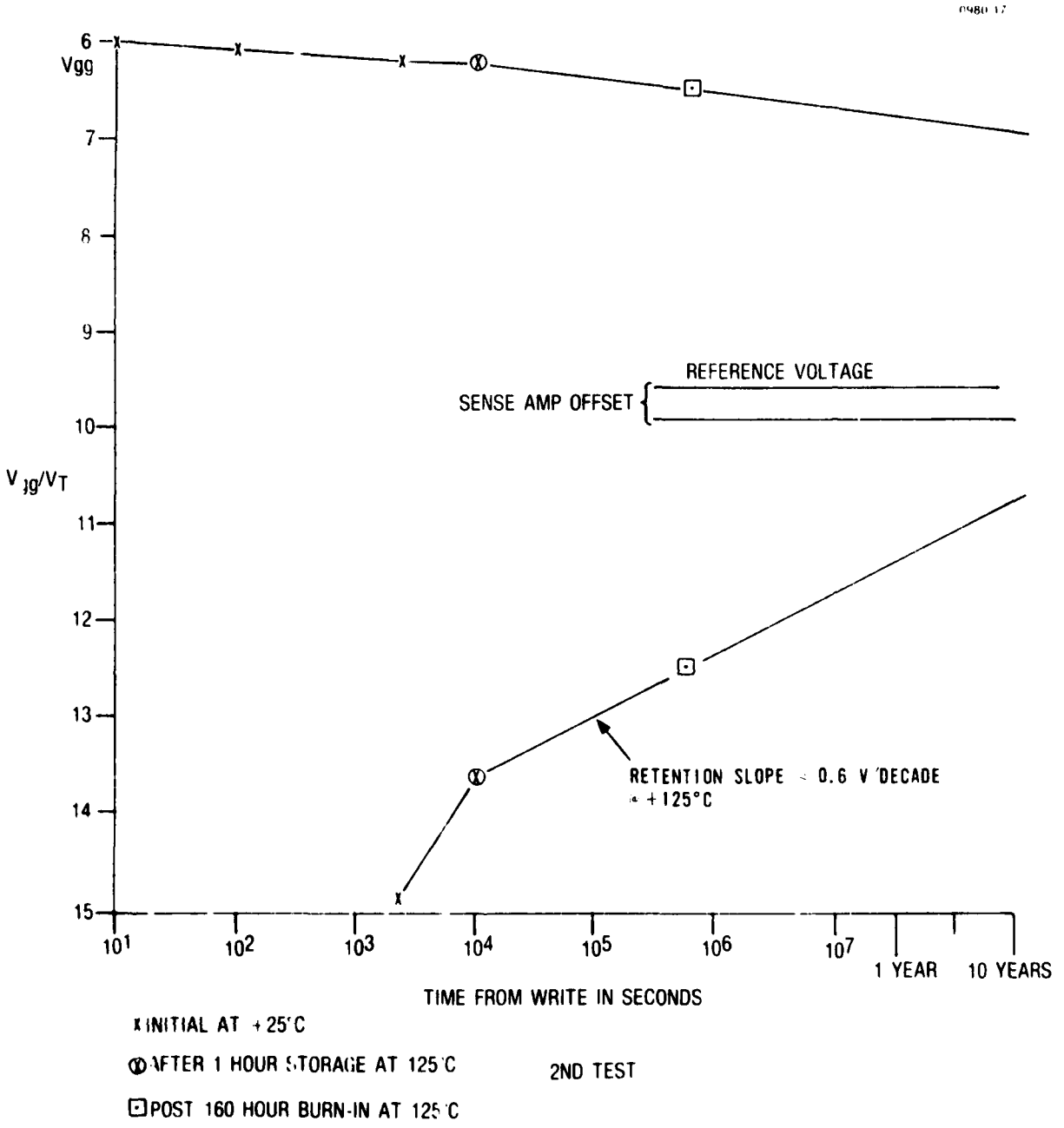


FIGURE 7-7. SECOND BURN-IN PERIOD FOR ER3400 DEVICE NO. 875

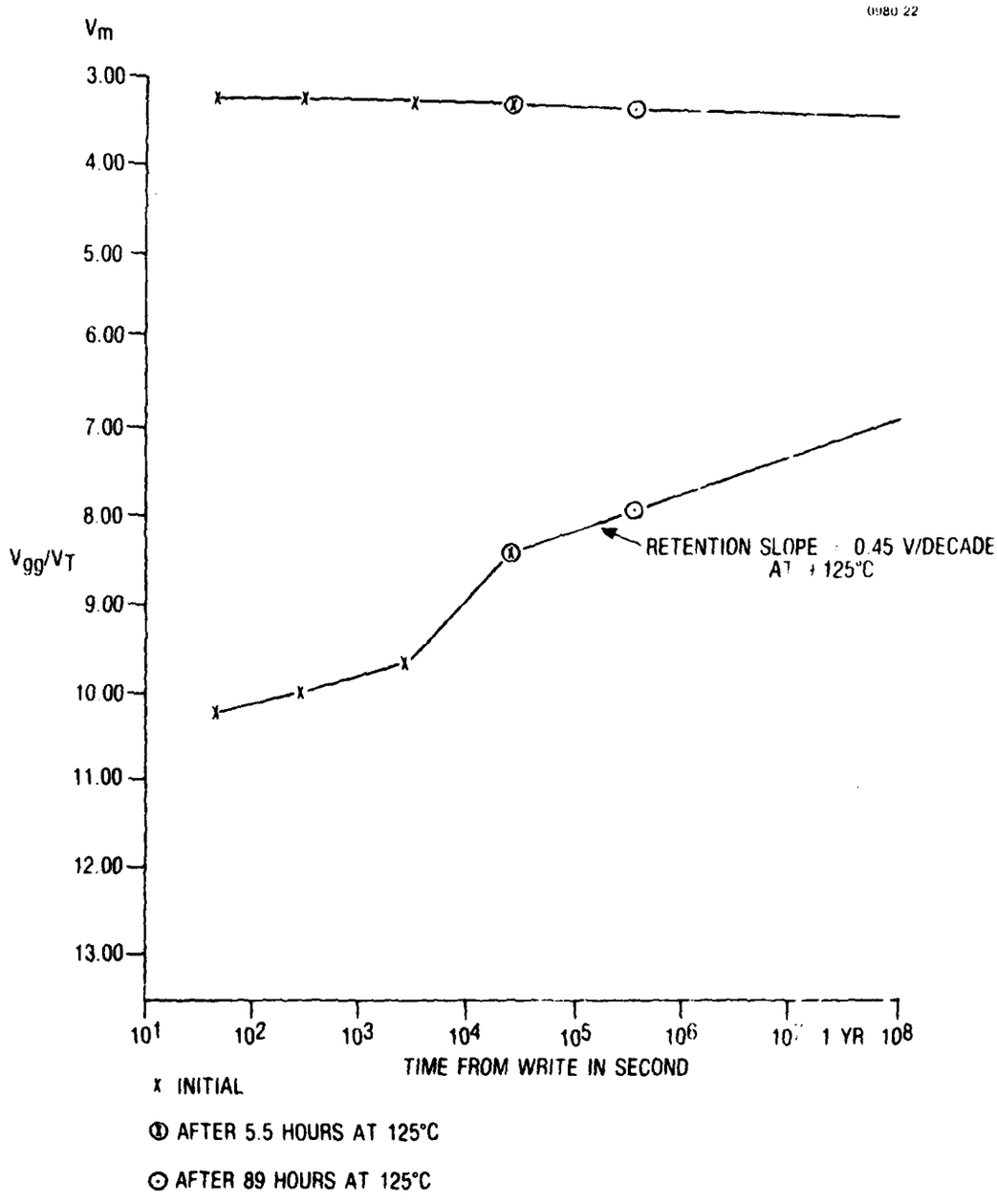


FIGURE 7-8. ER2810 (LPCVD NITRIDE) RETENTION PLOT AT +125°C FOR DEVICE NO. T1

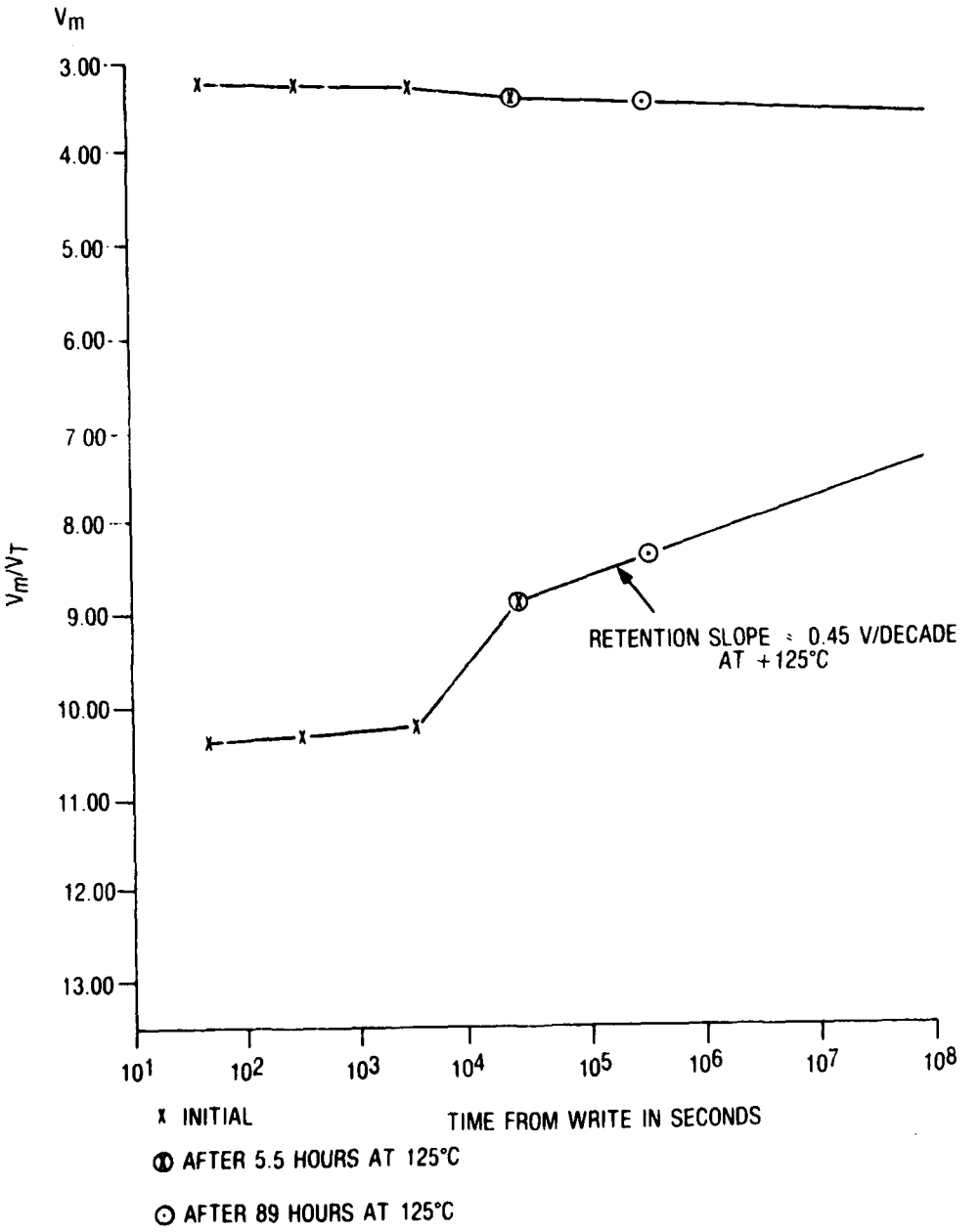
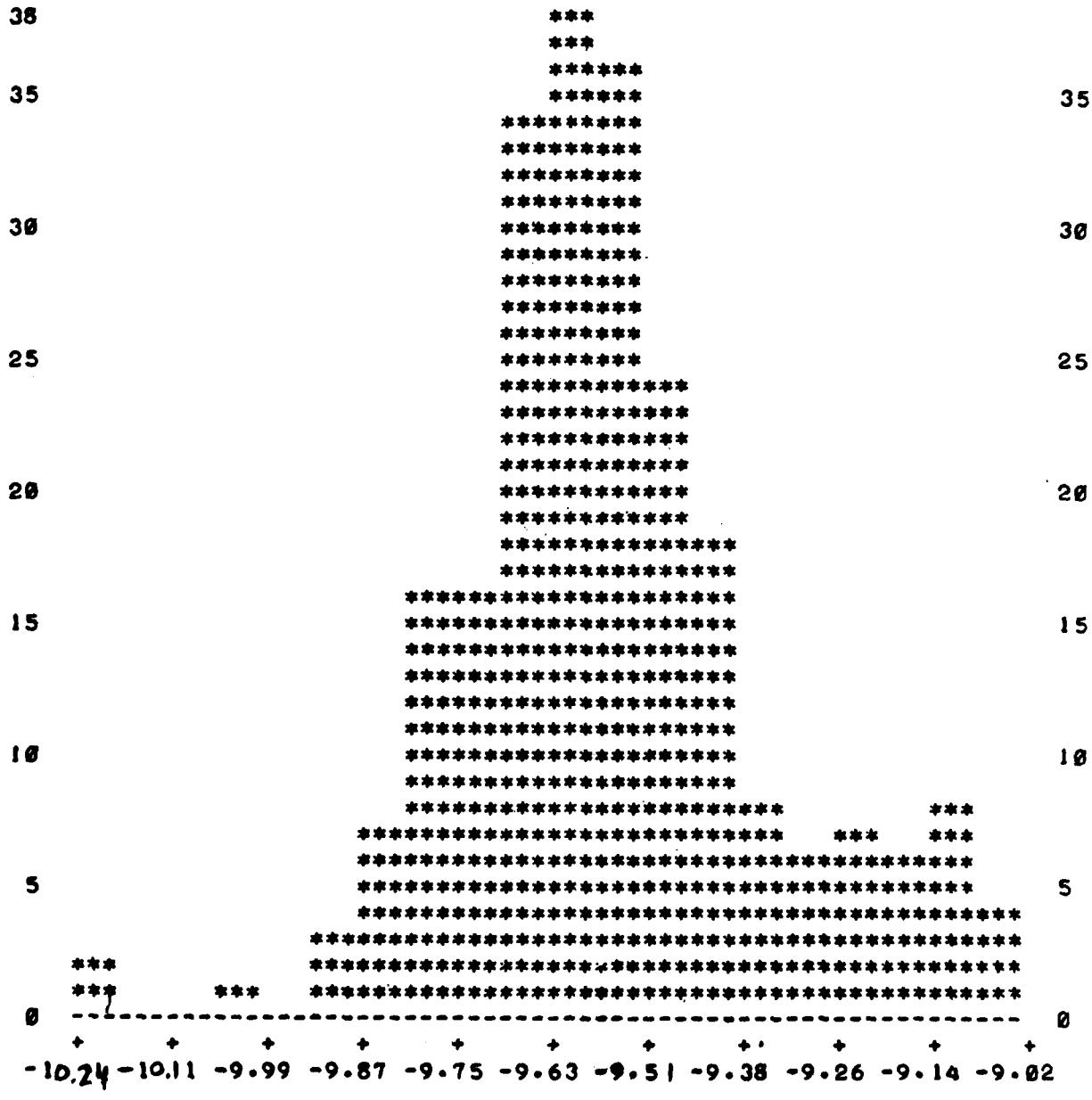


FIGURE 7-9. ER2810 (LPCVD NITRIDE) RETENTION PLOT AT +125°C FOR DEVICE NO. T9

234	NUMBER OF MEASUREMENTS
-9.54696581	MEAN
.197987368	ONE STANDARD DEVIATION
-10.24	MINIMUNVALUE
-9.02	MAXIMUM VALUE



REFERENCE VOLTAGE OF ALL TESTED MACI WAROMS
IN UNITS OF volts

FIGURE 7-10. INTERNAL REFERENCE VOLTAGE OF ALL ER3400/NCR2451 PARTS USED IN MACI PROGRAM

50	NUMBER OF MEASUREMENTS
-9.4628	MEAN
.196947333	ONE STANDARD DEVIATION
-9.76	MINIMUNVALUE
-9.02	MAXIMUM VALUE

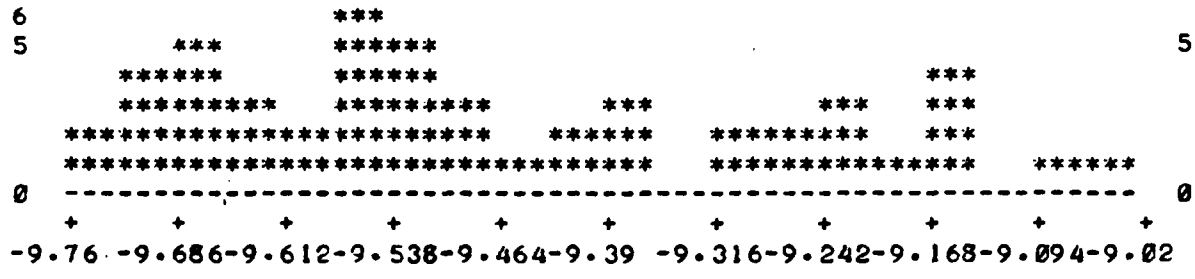


FIGURE 7-11. INTERNAL REFERENCE VOLTAGE DISTRIBUTION OF ALL ER3800/NCR2451 PARTS PASSING SCREEN TEST

50	NUMBER OF MEASUREMENTS
.278	MEAN
.050279221	ONE STANDARD DEVIATION
.15	MINIMUNVALUE
.38	MAXIMUM VALUE

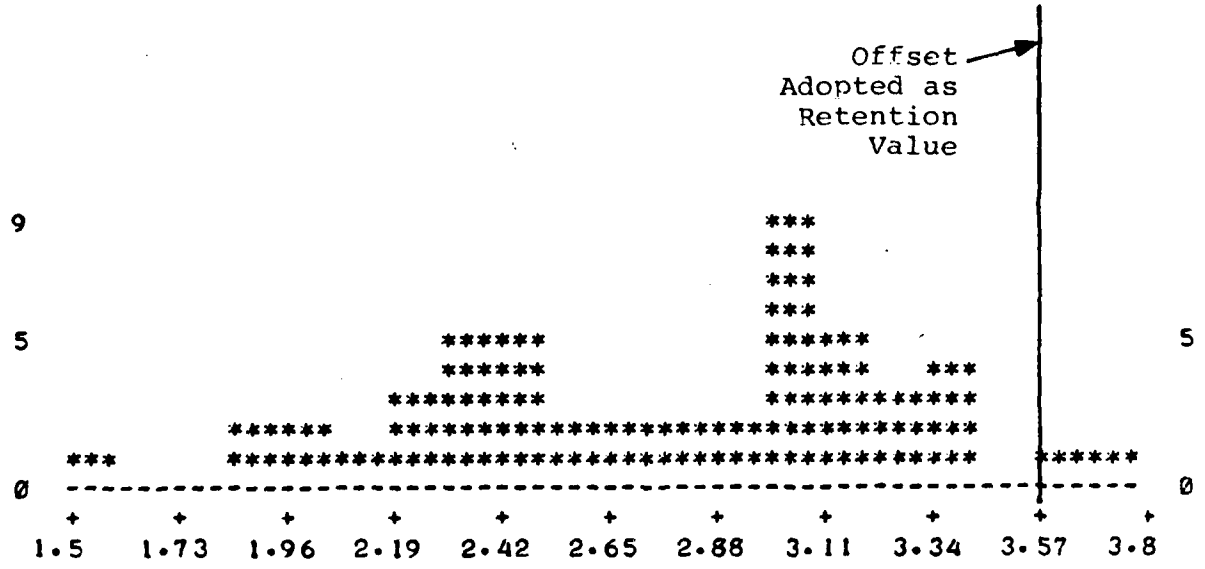


FIGURE 7-12. DISTRIBUTION OF ER3400/NCR2451 PARTS PASSING SCREEN TEST

233	NUMBER OF MEASUREMENTS
.243733905	MEAN
.0659448202	ONE STANDARD DEVIATION
-.03	MINIMUMVALUE
.59	MAXIMUM VALUE

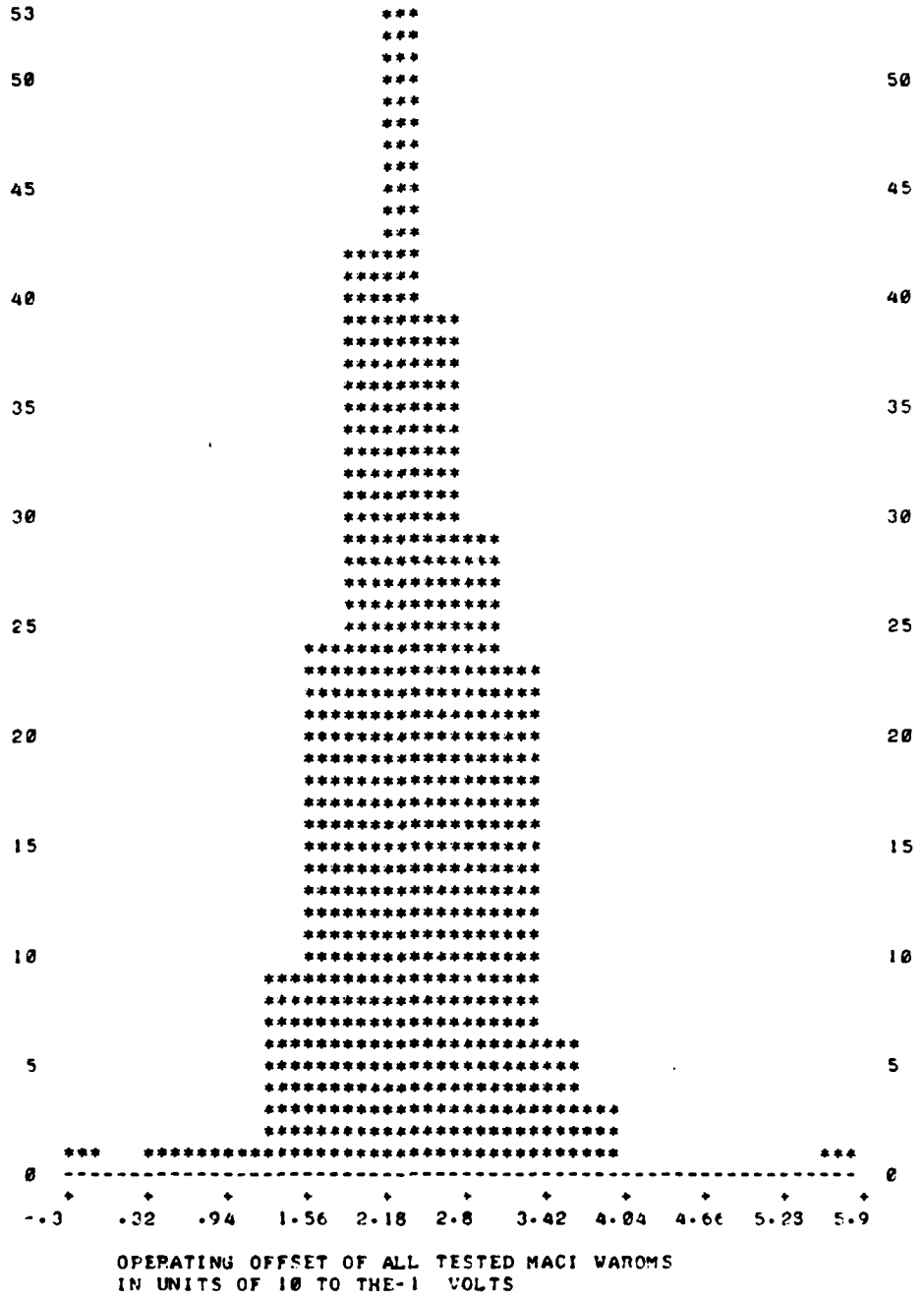


FIGURE 7-13. DISTRIBUTION OF ALL ER3400/NCR2451 MEASURED OFFSET VALUES FOR MACI PROGRAM

the intersection of the retention curve and a line drawn for the Reference Voltage minus the offset, a realistic prediction of the retention can be made.

7.1.4 D.C. Parameter Tests. These tests listed in Appendix A* of the Test Plan resulted in a loss of four parts as shown from Figure 7-1. Table 7-1 lists the results of input leakage and power supply current test at +25 degree C on all parts tested. Table 7-2 shows the results of these safe tests performed at +125 degree C which is much more rigorous for the leakage tests. Figure 7-14 shows the distribution of the measured values of IDD current in the de-selected state at +125 degree C. The distribution of this parameter in the selected state is shown in Figure 7-15 at +125 degree C. This shows that approximately 1/5 of the power of the device can be saved by being in the de-selected mode at +125 degree C.

The IGG current at +125 degree C is shown not to be a significant contributing factor in the device power dissipation at +125 degree C in Figure 7-16. Since Vgg is specified at +30 Vdc a typical, +125 degree C power consumption of 30 mw is seen.

Figures 7-17 and 7-18 show the Iss (Vss = +5V) current at +125 degree C in both the selected and de-selected modes for the 55 devices that had passed all previous screening.

Since the ER3400/NCR2451 devices under test in the MACI Program are specified for the commercial range, one parameter of particular interest at +125 degree C is the output voltage levels at specified load values. Figure 7-19 shows the distribution of parts tested for this parameter. As can be seen three parts failed this test. The mean value of all tested parts was 0.39 volts, well below the 0.5 volts specified. The output high voltage level distribution is shown in Figure 7-20 at +125 degree C showing all devices passing specified values.

At -55 degree C ditferent parameters become critical than at the high temperatures. Device power supply current increases signficantly as can be seen in Figures 7-21 through 7-25 at -55 degree C. Figures 7-21 and 7-22 examine the distribution of Idd (VDD = -13V) in both the de-selected and selected modes. De-selected devices show approximately a 40 percent reduction in power supply current from selected devices. Some devices operate very close to the specified maximum limit at low temperature (-27 ma). As can be seen, Igg current, while significantly increasing at -55 degree C (Figure 7-23), is still a minor contributor to device power requirements. Iss (Vss = +5V) current is shown in both de-selected and selected modes at -55 degree C.

*Appendix A and B omitted from this report. Interested parties may contact the contracting agency.

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C

DEVICE TEMP	VOH D0 VOH D1 VOH D2 VOH D3 VOLTS	VOL D0 VOL D1 VOL D2 VOL D3 VOLTS	ILC C0 ILC C1 U AMP	ILD D0 ILD D1 ILD D2 ILD D3 U AMP	IDD DS IDD S M AMP	IGG M AMP	ISS DS ISS S M AMP
778	4.305	0.305	-	-	8.270	1.3625	9.2625
25 C	4.335	0.210	-	-	10.475		10.675
7/2/80	4.330	0.270		-			
	4.315	0.295		-			
789	4.330	0.285	-	-	9.1525	1.4250	10.300
25 C	4.330	0.265	-	-	12.925		11.950
7/2/80	4.325	0.210		-			
	4.290	0.205		-			
788	4.335	0.205	-	-	8.8300	1.5400	9.9525
25 C	4.315	0.195	-	-	11.050		11.450
7/2/80	4.315	0.200	-	-			
	4.305	0.195		-			
787	4.360	0.235	-	-	8.6225	1.2100	9.5125
25 C	4.340	0.170	-	-	13.100		11.725
7/2/80	4.345	0.180		-			
	4.310	0.210		-			
786	4.300	0.255	-	-	9.0575	1.6025	10.325
25 C	4.295	0.215	-	-	11.825		12.050
7/2/80	4.280	0.210		-			
	4.270	0.270		-			
785	4.290	0.215	-	-	8.6575	1.4100	9.7925
25 C	4.300	0.220	-	-	10.900		11.300
7/2/80	4.290	0.205		-			
	4.250	0.205		-			
783	4.325	0.195	-	-	9.1425	1.3025	10.1400
25 C	4.340	0.195	-	-	12.900		14.125
7/2/80	4.340	0.190		-			
	4.305	0.185		-			
782	4.320	0.250	-	-	9.0625	1.8900	10.525
25 C	4.315	0.195	-	-	12.875		13.875
7/2/80	4.300	0.220		-			
	4.305	0.210		-			
803	4.340	0.220	-	-	9.6875	1.5650	10.675
25 C	4.345	0.210	-	-	13.600		14.200
7/2/80	4.320	0.210		-			
	4.340	0.175		-			

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE 25 C DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S		
799	4.340	0.195	-	-	9.4675	1.3400	10.500
25 C	4.310	0.195	-	-	13.600		14.275
7/2/80	4.330	0.195		-			
	4.325	0.190		-			
798	4.345	0.190	-	-	9.1050	1.3400	10.1000
25C	4.345	0.185	-	-	12.925		14.325
7/2/80	4.345	0.185		-			
	4.335	0.175		-			
????	4.365	0.185	-	-	9.6825	1.5550	10.675
25 C ~~000005~~	4.345	0.195	-	-	13.600		12.675
7/2/80	4.315	0.205		-			
	4.335	0.215		-			
811	4.330	0.200	-	-	8.7400	1.0725	9.6300
25 C	4.325	0.205	-	-	12.625		13.100
7/2/80	4.320	0.195		-			
	4.310	0.190		-			
//							
821	4.275	4.245	4.265	4.270			
25 C	0.255	0.225	0.275	0.225			
7/3/80	0.02	0.02					
	0.02	0.02	0.02	0.02			
	8.773	13.875	1.335	9.870	11.300		
822	4.380	4.375	4.365	4.365			
25 C	0.200	0.240	0.185	0.180			
7/3/80	0.02	0.02					
	0.02	0.02	0.02	0.02			
	9.4125	13.600	1.218	10.400	14.450		
826	4.330	4.330	4.330	4.315			
25 C	0.225	0.225	0.220	0.210			
7/3/80	0.02	0.02					
	0.02	0.02	0.02	0.02			
	9.165	13.100	1.445	10.275	13.800		
828	4.300	4.290	4.310	4.330			
25 C	0.250	0.220	0.265	0.270			
7/3/80	0.02	0.02					
	0.02	26.825	0.02	0.02			
	8.295	10.400	1.365	9.333	10.650		

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
829	4.250	4.240	4.275	4.265	
7/3/80	0.305	0.205	0.235	0.210	
25 C	0.02	0.02			
	0.02	0.02	0.02	0.02	
	8.415	10.875	1.370	9.480	10.925
831	4.350	4.345	4.350	4.305	
7/3/80	0.210	0.245	0.190	0.210	
25 C	0.02	0.02			
	0.02	0.02	0.02	0.02	
	8.823	13.475	1.500	9.918	11.500
833	4.230	4.290	4.275	4.235	
7/3/80	0.250	0.210	0.225	0.205	
25 C	0.02	0.02			
	0.02	0.02	0.02	0.02	
	8.608	11.450	1.508	9.783	10.975
834	4.315	4.315	4.305	4.285	
7/3/80	0.215	0.270	0.245	0.285	
25 C	0.02	0.02			
	0.02	0.02	0.02	0.02	
	8.435	10.550	1.498	9.530	10.925
835	4.330	4.340	4.330	4.325	
25 C	0.185	0.175	0.215	0.215	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	9.197	13.72	1.382	10.072	14.450
840	4.350	4.345	4.350	4.335	
25 C	0.185	0.180	0.185	0.170	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	9.055	12.900	1.475	10.085	13.550
841	4.325	4.305	4.315	4.295	
25 C	0.195	0.180	0.175	0.185	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	9.307	13.300	1.622	10.475	14.050

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

>PR
UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
25 C	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
844	4.345	4.375	4.305	4.355	
25 C	0.200	(0.190	0.190	0.180	
7/3/80	0.029	0.018			
	0.021	0.021	0.021	0.021	
	9.490	13.475	1.600	10.500	12.625
845	4.325	4.330	4.320	4.310	
25 C	0.245	0.205	0.200	(0.215	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.748	11.000	1.545	9.917	11.225
(846	4.330	4.325	4.320	4.310	
25 C	0.268	0.195	0.218	0.185	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.880	13.700	1.467	9.995	12.075
847	4.365	4.380	4.385	4.330	
25 C	0.185	0.200	0.255	0.170	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.727	11.000	1.295	9.720	11.525
849	4.340	4.335	4.310	4.290	
25 C	0.290	0.215	0.225	0.265	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.618	12.825	1.470	9.723	11.450
851	4.335	4.345	4.340	4.320	
25 C	0.200	0.195	0.190	0.195	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.743	13.275	1.505	9.833	11.425
852	4.290	4.290	4.285	4.275	
25 C	0.295	0.285	4.215	0.265	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.467	12.900	1.395	9.583	10.975

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
853	4.350	4.345	4.315	4.325	
25 C	0.190	0.195	0.185	0.200	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	9.855	13.750	1.587	10.800	14.300
854	4.365	4.355	4.360	4.350	
"25 C	0.205	0.230	0.225	0.202	
7/3/80	0.021	0.018			
	0.021	0.021	0.021	0.021	
	8.558	30.850	1.523	9.650	11.125

END OF"TESTING 7/3/80
//

861	4.280	4.300	4.305	4.295	
25 C	.250	.185	.185	.185	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.148	12.850	1.455	10.168	13.975
862	4.305	4.300	4.290	4.290	
25 C	.240	.250	.220	.210	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.555	12.500	1.2125	9.528	11.950
865	4.330	4.320	4.310	4.305	
25 C	.205	.210	.200	.250	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.855	13.250	1.548	9.953	11.875
868	4.260	4.260	4.275	4.250	
25 C	.310	.290	.270	.275	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.588	12.300	2.010	10.163	14.050

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
874	4.320	4.310	4.320	4.295	
25 C	.225	.230	.220	.210	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.038	13.125	1.570	10.190	12.100
881	4.320	4.345	0.285	0.210	
25 C	.215	.305	.205	.210	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	7.788	13.475	1.158	8.723	9.798
876	4.245	4.310	4.250	4.245	
25 C	.245	.245	.245	.255	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.293	14.625	1.300	9.375	10.725
890	4.340	4.345	4.345	4.330	
25 C	.190	.180	.195	.170	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.993	12.800	1.480	10.013	13.425
891	4.310	4.295	4.260	4.240	
25 C	.205	.205	.200	.185	
7/7/80	0.020	0.018			
	0.015	0.010	0.013	0.014	
	8.028	9.743	1.385	9.080	10.143
892	4.400	4.395	4.390	4.390	
25 C	.180	.225	.170	.160	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.048	13.500	1.360	10.035	12.600
893	4.295	4.290	4.305	4.295	
25 C	.215	.260	.245	.225	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.703	10.925	1.665	9.918	11.450

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
894	4.375	4.370	4.330	4.365	
25 C	.185	.170	.165	.165	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.963	13.700	1.290	9.918	14.475
895	4.275	4.315	4.300	4.295	
25 C	.260	.245	.230	.245	
7/7/80	0.021	0.015			
	0.021	0.021	0.021	0.021	
	8.390	11.650	1.508	9.478	10.850
896	4.320	4.295	4.310	4.310	
25 C	.220	.250	.245	.250	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.318	13.250	1.358	9.348	10.800
897	4.290	4.290	4.275	4.275	
25 C	.245	.230	.230	.230	
7/7/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.703	12.450	1.665	10.008	13.250
898	4.315	4.330	4.315	4.325	
25 C	0.210	0.215	0.235	0.200	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.680	13.175	1.503	9.793	11.300
899	4.350	4.340	4.310	4.335	
25 C	0.200	0.200	0.190	0.220	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.625	11.375	1.365	9.655	11.575
900	4.315	4.325	4.325	4.300	
25 C	0.200	0.210	0.185	0.210	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.905	13.175	1.358	9.908	11.675

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
901	4.315	4.310	4.300	4.295	
25 C	0.240	0.205	0.240	0.255	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.475	12.425	1.363	9.4975	10.875
902	4.325	4.330	4.330	4.315	
25 C	0.220	0.220	0.310	0.195	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	8.580	12.225	1.523	9.680	10.975
2001	4.320	4.305	4.300	4.295	
25 C	0.210	0.180	0.180	0.175	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	10.425	13.475	2.193	12.250	14.675
2002	4.295	4.285	4.270	4.280	
25 C	0.185	0.215	0.180	0.180	
Z					
	0.021	0.021	0.021	0.021	
	10.275	13.625	2.145	12.050	15.025
2003	4.325	4.315	4.305	4.295	
25 C	0.230	0.185	0.175	0.170	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	10.325	13.750	2.248	12.225	14.950
2005	4.315	4.315	4.265	4.300	
25 C	0.190	0.185	0.185	0.190	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.838	13.475	2.130	11.700	13.675
2006	4.325	4.305	4.305	4.270	
25 C	0.195	0.215	0.185	0.210	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.968	14.600	2.080	11.775	13.375

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
2007	4.320	4.290	4.305	4.295	
25 C	0.215	0.205	0.175	0.170	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	10.500	14.050	2.240	12.375	15.525
2008	4.280	4.305	4.295	4.300	
25 C	0.185	0.200	0.180	0.245	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	10.085	14.250	2.068	11.825	14.300
2009	4.310	4.280	4.290	4.295	
25 C	0.190	0.180	0.190	0.180	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.950	12.975	2.0525	11.700	13.800
2010	4.320	4.310	4.300	4.310	
25 C	0.190	0.240	0.195	0.225	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	10.425	13.800	2.178	12.225	15.025
2011	4.305	4.305	4.305	4.300	
25 C	0.240	0.210	0.180	0.250	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.640	14.650	2.022	11.425	12.775
2012	4.295	4.285	4.285	4.270	
25 C	0.195	0.185	0.185	0.190	
7/8/80	0.020	0.018			
	0.021	0.021	0.021	0.021	
	9.633	12.050	1.945	11.325	13.250
2013	4.315	4.320	4.305	4.285	
25 C	0.185	0.205	0.175	0.180	
7/8/80	0.021	0.019			
	0.022	0.022	0.022	0.022	
	10.045	13.425	2.145	11.875	14.425

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
2014 25 C 7/8/80	4.330 0.190 0.021 0.022 10.022	4.310 0.235 0.019 0.022 13.325	4.280 0.185 0.022 2.028	4.300 0.185 0.022 11.800	14.325
2015 25 C 7/8/80	4.315 0.185 0.021 0.022 10.163	4.305 0.185 0.019 0.022 14.200	4.300 0.235 0.022 2.120	4.295 0.170 0.022 11.975	14.325
2016 25 C 7/8/80	4.320 0.210 0.021 0.022 10.475	4.300 0.190 0.019 0.022 14.150	4.300 0.185 0.022 2.167	4.250 0.250 0.022 12.275	14.825
2018 25 C 7/8/80	4.265 0.210 0.021 0.022 8.848	4.245 0.205 0.019 0.022 13.125	4.250 0.215 0.022 1.870	4.280 0.230 0.022 10.500	11.875
2019 25 C 7/8/80	4.280 0.195 0.021 0.022 10.325	4.295 0.235 0.019 0.022 13.675	4.285 0.190 0.022 2.243	4.280 0.195 0.022 12.325	15.050
2020 25 C 7/8/80	4.290 0.190 0.021 0.022 9.870	4.300 0.265 0.019 0.022 14.800	4.290 0.185 0.022 2.135	4.275 0.190 0.022 11.775	13.625
2022 25 C 7/8/80	4.325 0.175 0.021 0.022 10.208	4.320 0.185 0.019 0.022 13.675	4.310 0.190 0.022 2.158	4.270 0.165 0.022 12.100	15.025

TABLE 7-1. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 25°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
2023 25 C 7/8/80	4.320 0.180 0.021 0.022 10.158	4.300 0.215 0.019 0.022 13.000	4.300 0.175 0.022 2.133	4.305 0.205 0.022 12.100	14.575
2024 25 C 7/8/80	4.305 0.185 0.021 0.022 10.275	4.300 0.200 0.019 0.022 13.625	4.285 0.220 0.022 2.183	4.270 0.225 0.022 12.150	15.025
2026 25 C 7/8/80	4.345 0.205 0.021 0.022 10.198	4.315 0.180 0.015 0.022 14.025	4.305 0.200 0.022 2.233	4.315 0.185 0.022 12.125	14.025
871 25 C 7/8/80	4.320 0.205 0.021 0.022 8.940	4.320 0.205 0.019 0.022 11.425	4.280 0.210 0.022 1.678	4.310 0.205 0.022 10.140	11.825
880 25 C 7/8/80	4.305 0.310 0.021 0.022 8.523	4.305 0.205 0.019 0.022 12.650	4.290 0.240 0.022 1.280	4.255 0.205 0.022 9.520	10.900

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
782	4.130	4.150	4.110	4.095	
125 C	0.370	0.325	0.365	0.365	
7-8-80	0.031	0.022			
	0.045	0.043	0.043	0.045	
	6.595	8.665	1.398	7.538	9.655
783	4.135	4.130	4.125	4.130	
125 C	0.380	0.370	0.365	0.370	
7-8-80	0.024	0.019			
	0.034	0.035	0.035	0.035	
	6.648	8.705	0.874	7.358	8.938
785	4.070	4.065	4.065	4.050	
125 C	0.450	0.435	0.435	0.440	
7-9-80	0.023	0.019			
	0.033	0.032	0.032	0.032	
	6.197	7.640	0.952	7.033	8.343
787	4.220	4.175	4.185	4.150	
125 C	0.345	0.330	0.345	0.280	
7-9-80	0.023	0.019			
	0.032	0.032	0.032	0.032	
	6.235	8.015	0.765	6.880	8.540
798	4.145	4.135	4.140	4.125	
125 C	0.370	0.355	0.350	0.345	
7-9-80	0.024	0.019			
	0.036	0.037	0.037	0.037	
	6.615	8.373	0.912	7.345	8.935
799	4.180	4.155	4.160	4.155	
125 C	0.330	0.330	0.330	0.325	
7-9-80	0.024	0.019			
	0.039	0.042	0.042	0.041	
	6.913	9.185	1.415	7.628	9.783
803	4.180	4.180	4.145	4.170	
125 C	0.325	0.345	0.325	0.305	
7-9-80	0.024	0.019			
	0.034	0.035	0.038	0.034	
	7.113	0.9.110	1.060	7.790	10.003

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
811	4.140	4.130	4.110	4.105	
125 C	0.355	0.345	0.345	0.340	
7-9-80	0.033	0.023			
	0.049	0.052	0.053	0.051	
	6.337	8.425	0.782	6.998	10.025
821	4.080	4.105	4.100	4.060	
125 C	0.420	0.420	0.420	0.420	
7-9-80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.300	7.665	0.898	7.105	8.335
822	4.185	4.185	4.175	4.175	
125 C	0.325	0.325	0.315	0.315	
7-9-80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.855	9.175	0.812	7.530	9.438
826	4.150	4.155	4.155	4.145	
125 C	0.350	0.340	0.330	0.330	
7-9-80	0.024	0.019			
	0.039	0.039	0.040	0.040	
	6.740	8.815	1.485	7.508	9.630
828	4.095	4.080	4.085	4.075	
125 C	0.390	0.385	0.375	0.460	
7-9-80	0.024	0.019			
	0.029	26.50	0.029	0.029	
	5.990	7.250	0.895	6.715	7.853
831	4.170	4.135	4.155	4.125	
125 C	0.385	0.365	0.360	0.360	
7-9-80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.318	7.730	0.943	7.090	8.373
833	4.050	4.045	4.045	4.035	
125 C	0.455	0.485	0.375	0.415	
7-9-80	0.022	0.017			
	0.030	0.030	0.034	0.030	
	6.218	7.335	0.985	7.070	8.063

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
835	4.165	4.155	4.150	4.150	
125 C	0.335	0.325	0.325	0.325	
7-9-80	0.024	0.019			
	0.034	0.035	0.036	0.035	
	6.778	8.268	0.874	7.358	8.793
840	4.155	4.160	4.160	4.150	
125 C	0.335	0.330	0.325	0.325	
7-9-80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.555	8.535	0.967	7.263	8.888
"					
841	4.155	4.145	4.145	4.145	
125 C	0.350	0.345	0.345	0.330	
7/9/80	0.024	0.019			
	0.037	0.039	0.039	0.038	
	6.830	8.938	1.098	7.640	9.655
844	4.155	4.170	4.155	4.155	
125 C	0.330	0.305	ZX310	0.300	
7/9/80	0.022	0.019			
	0.032	0.032	0.032	0.031	
	7.040	8.968	1.085	7.705	9.640
846	4.125	4.150	4.110	4.105	
125 C	0.405	0.360	0.390	0.400	
7/9/80	0.024	0.019			
	0.031	0.030	0.030	0.031	
	6.400	8.243	0.949	7.188	8.878
849	4.110	4.120	4.110	4.110	
125 C	0.430	0.465	0.405	0.425	
7/9/80	0.023	0.017			
	0.031	0.032	0.032	0.032	
	6.198	7.730	0.970	7.015	8.415
851	4.140	4.125	4.130	4.110	
125 C	0.365	0.355	0.360	0.350	
7/9/80	0.024	0.019			
	0.030	0.031	0.030	0.031	
	6.280	7.675	0.958	7.063	8.335

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
853	4.175	4.175	4.165	4.170	
125 C	0.310	0.300	0.310	0.290	
7/9/80	0.024	0.019			
	0.035	0.035	0.034	0.034	
	7.325	9.165	1.063	7.933	9.743
854	4.130	4.145	4.140	4.125	
125 C	0.430	0.415	0.405	0.410	
7/9/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.195	7.585	0.959	6.983	8.250
855	4.090	4.100	4.080	4.07	
125 C	0.390	0.365	0.355	0.385	
7/9/80	0.023	0.015			
	0.030	0.030	0.030	0.030	
	6.353	7.558	0.969	7.143	8.278
858	4.140	4.155	4.095	4.095	
125 C	0.410	0.405	0.400	0.385	
7/10/80	0.023	0.017			
	0.033	0.033	0.033	0.033	
	6.228	7.790	0.992	7.065	8.505
861	4.120	4.110	4.115	4.110	
125 C	0.375	0.365	0.360	0.365	
7/9/80	0.024	0.019			
	0.039	0.039	0.039	0.039	
	6.633	8.615	1.000	7.345	8.985
862	4.105	4.075	4.065	4.040	
125 C	0.765	0.625	0.565	0.530	
7/10/80	0.030	0.023			
	0.048	0.052	0.053	0.056	
	6.2375	8.028	0.873	6.953	8.525
868	4.085	4.095	4.090	4.065	
125 C	0.420	0.400	0.390	0.390	
7/10/80	0.025	0.021			
	0.043	0.045	0.046	0.045	
	6.288	8.130	1.350	7.440	8.910

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
871	4.105	4.105	4.105	4.105	
125 C	0.415	0.395	0.405	0.405	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.438	7.950	1.072	7.310	8.698
876	4.075	4.145	4.075	4.050	
125 C	0.330	0.500	0.650	0.665	
7/10/80	0.024	0.019			
	0.031	0.031	0.031	0.030	
	5.995	7.093	0.862	6.778	7.785
880	4.090	4.125	4.100	4.130	
125 C	0.450	0.430	0.435	0.305	
7/10/80	0.024	0.019			
	0.031	0.031	0.031	0.030	
	6.150	7.408	0.779	6.843	7.968
890	4.150	4.155	4.155	4.145	
125 C	0.345	0.325	0.315	0.325	
7/10/80	0.024	0.019			
	0.032	0.032	0.032	0.031	
	6.558	8.595	0.978	7.288	8.860
//					
892	4.210	4.205	4.200	4.200	
125 C	0.355	0.335	0.325	0.325	0.330
7/10/80	0.026	0.021			
	0.039	0.040	0.041	0.041	
	6.598	8.568	0.878	7.303	9.103
893	4.070	4.085	4.080	4.080	
125 C	0.440	0.425	0.410	0.410	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.283	7.693	1.083	7.168	8.455
894	4.185	4.185	4.175	4.155	
125 C	0.345	0.320	0.325	0.330	
7/10/80	0.024	0.019			
	0.036	0.037	0.037	0.037	
	6.538	8.440	0.818	7.208	8.983

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
895	4.090	4.090	4.085	4.075	
125 C	0.450	0.435	0.430	0.425	
7/10/80	0.023	0.015			
	0.031	0.031	0.031	0.031	
	6.073	7.358	0.958	6.878	8.015
897	4.090	4.100	4.095	4.090	
125 C	0.395	0.385	0.385	0.375	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.390	8.443	1.085	7.358	8.795
900	4.130	4.120	4.115	4.105	
125 C	0.385	0.370	0.370	0.365	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	6.425	8.065	0.828	7.118	8.608
2001	4.170	4.165	4.155	4.165	
125 C	0.320	0.305	0.290	0.350	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.663	9.233	1.723	8.965	10.475
2002	4.160	4.145	4.120	4.100	
125 C	0.340	0.300	0.335	0.315	
7/10/80	0.024	0.019			
	0.033	0.030	0.029	0.029	
	7.555	9.213	1.688	8.850	10.475
2003	4.180	4.190	4.185	4.185	
125 C	0.345	0.300	0.265	0.255	
7/10/80	0.024	0.019			
	0.031	0.029	0.030	0.029	
	7.598	9.298	1.750	8.980	10.625
2005	4.190	4.170	4.150	4.145	
125 C	0.295	0.370	0.370	0.285	
7/10/80	0.021	0.019			
	0.032	0.030	0.031	0.031	
	7.185	8.760	1.678	8.503	9.950

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
2006	4.190	4.140	4.165	4.140	
125 C	0.385	0.285	0.290	0.280	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.238	8.730	1.613	8.530	9.893
2007	4.195	4.170	4.135	4.155	
125 C	0.380	0.330	0.325	0.285	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.658	10.060	1.753	9.020	10.750
2008	4.180	4.155	4.155	4.160	
125 C	0.330	0.365	0.290	0.295	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.413	9.045	1.615	8.670	10.180
2009	4.185	4.165	4.125	4.115	
125 C	0.370	0.290	0.325	0.290	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.333	8.890	1.620	8.598	10.030
2010	4.185	4.165	4.155	4.125	
125 C	0.305	0.295	0.345	0.275	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.658	9.320	1.723	8.995	10.625
2011	4.190	4.175	4.180	4.110	
125 C	0.280	0.295	0.370	0.275	
7/10/80	0.024	0.019			
	0.033	0.033	0.033	0.033	
	7.038	8.373	1.573	8.313	9.525
2012	4.150	4.160	4.090	4.145	
125 C	0.285	0.270	0.330	0.275	
7-10-80	0.024	0.019			
	0.032	0.032	0.032	0.032	
	7.095	8.730	1.503	8.308	9.800

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE TEMP DATE	VOH D0 VOL D0 ILC C0 ILD D0 IDD DS	VOH D1 VOL D1 ILC C1 ILD D1 IDD S	VOH D2 VOL D2 ILD D2 IGG	VOH D3 VOL D3 ILD D3 ISS DS	ISS S
2013	4.175	4.165	4.155	4.150	
125 C	0.325	0.305	0.315	0.305	
7-10-80	0.024	0.019			
	0.032	0.032	0.032	0.032	
	7.335	8.970	1.718	8.658	10.208
2014	4.205	4.180	4.165	4.165	
125 C	0.310	0.270	0.365	0.360	
7-10-80	0.024	0.019			
	0.029	0.030	0.030	0.029	
	7.323	9.053	1.550	8.598	10.200
2015	4.175	4.160	4.130	4.145	
125 C	0.365	0.355	0.355	0.345	
7-10-80	0.024	0.019			
	0.032	0.032	0.032	0.032	
	7.405	9.048	1.650	8.725	10.205
2016	4.170	4.130	4.130	4.125	
125 C	0.335	0.315	0.325	0.350	
7-10-80	0.024	0.019			
	0.032	0.032	0.032	0.032	
	7.635	9.247	1.698	8.940	10.500
2018	4.085	4.120	4.110	4.110	
125 C	0.345	0.430	0.330	0.385	
7-10-80	0.024	0.019			
	0.031	0.030	0.029	0.028	
	6.490	7.805	1.433	7.643	8.855
2019	4.115	4.110	4.135	4.110	
125 C	0.295	0.305	0.300	0.335	
7-11-80	0.023	0.019			
	0.032	0.032	0.032	0.032	
	7.535	9.178	1.740	9.053	10.600
2020	4.145	4.155	4.145	4.110	
125 C	0.295	0.320	0.350	0.390	
7-11-80	0.023	0.019			
	0.032	0.031	0.029	0.029	
	7.173	8.660	1.578	8.518	9.895

TABLE 7-2. INPUT LEAKAGE AND POWER SUPPLY CURRENT AT 125°C (Continued)

UNITS: VOLTS; INPUT LEAKAGE-MICROAMPERES; SUPPLY CURRENT-MILLIAMPERES

DEVICE	VOH D0	VOH D1	VOH D2	VOH D3	
TEMP	VOL D0	VOL D1	VOL D2	VOL D3	
DATE	ILC C0	ILC C1			
	ILD D0	ILD D1	ILD D2	ILD D3	
	IDD DS	IDD S	IGG	ISS DS	ISS S
2022	4.170	4.135	4.130	4.130	
125 C	0.310	0.335	0.335	0.295	
7-11-80	0.023	0.019			
	0.030	0.030	0.030	0.029	
	7.420	9.125	1.670	8.763	10.500
2023	4.175	4.155	4.125	4.155	
125 C	0.325	0.290	0.345	0.280	
7-11-80	0.023	0.019			
	0.032	0.032	0.032	0.032	
	7.395	9.153	1.568	8.740	10.350
2024	4.170	4.160	4.135	4.130	
125 C	0.350	0.285	0.305	0.290	
7-11-80	0.023	0.019			
	0.032	0.032	0.032	0.032	
	7.513	9.175	1.713	8.860	10.525
2026	4.180	4.140	4.155	4.145	
125 C	0.355	0.370	0.345	0.340	
7-11-80	0.023	0.017			
	0.040	0.039	0.039	0.036	
	7.430	9.005	1.783	8.838	10.300

```
55                  NUMBER OF MEASUREMENTS
6.52745454          MEAN
.454649639          ONE STANDARD DEVIATION
5.9                 MINIMUNVALUE
7.56                MAXIMUM VALUE
```

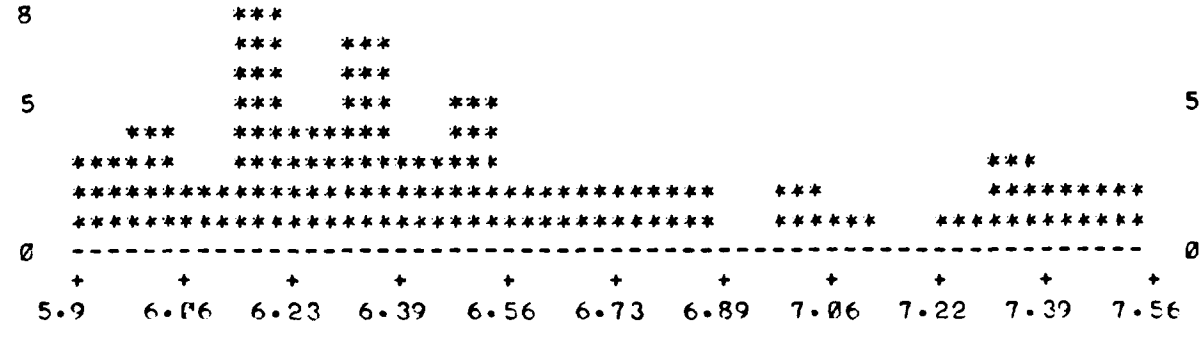


FIGURE 7-14. DISTRIBUTION OF MEASURED IDD (DE-SELECTED) VALUES AT +125°C

```
55                  NUMBER OF MEASUREMENTS
8.11018182          MEAN
.65406835           ONE STANDARD DEVIATION
7.16                MINIMUNVALUE
9.21                MAXIMUM VALUE
```

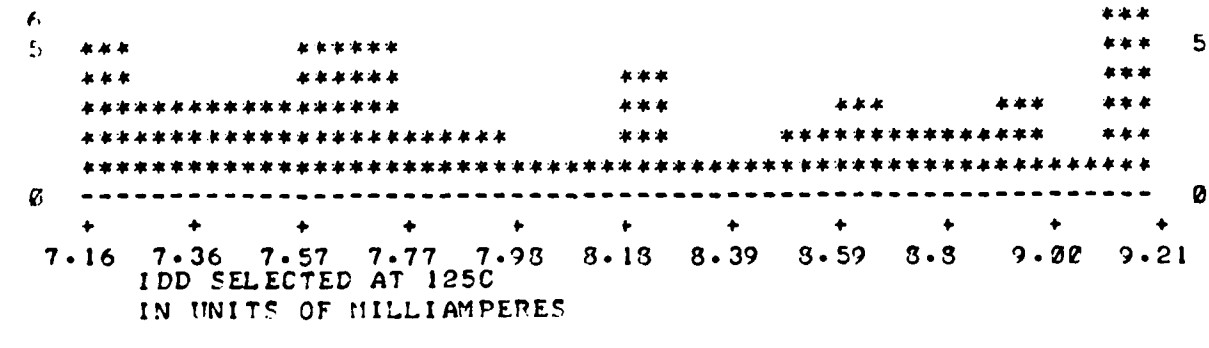


FIGURE 7-15. DISTRIBUTION OF MEASURED IDD (SELECTED) VALUES AT +125°C

54	NUMBER OF MEASUREMENTS
1.11592593	MEAN
.277211768	ONE STANDARD DEVIATION
.78	MINIMUNVALUE
1.8	MAXIMUM VALUE

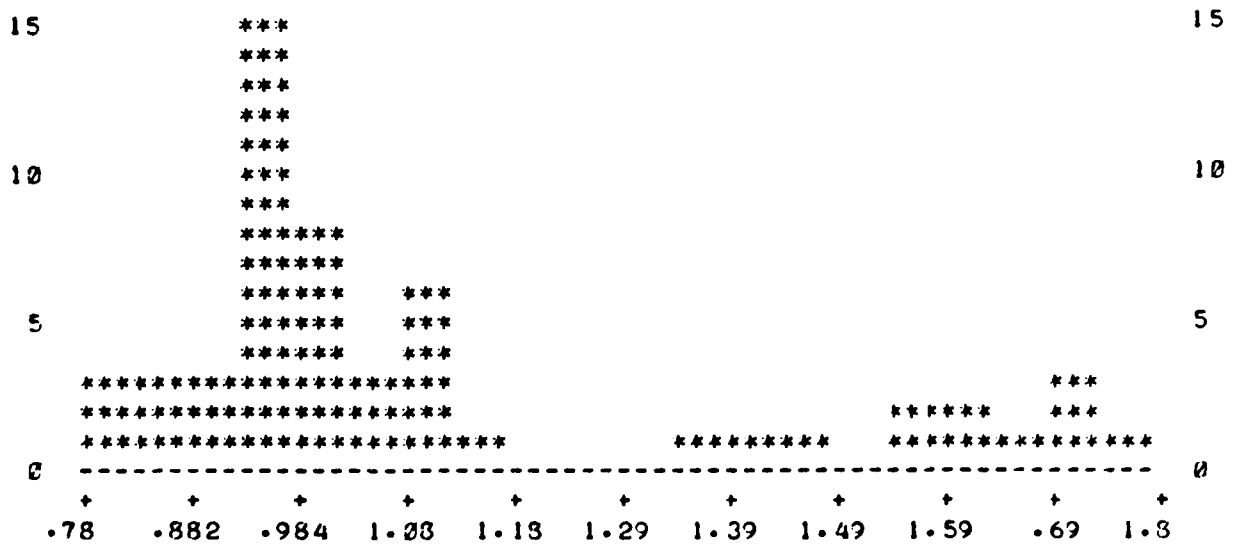


FIGURE 7-16. DISTRIBUTION OF MEASURED VALUE OF IGG AT +125°C

```
55                    NUMBER OF MEASUREMENTS
7.40581818            MEAN
.601584795            ONE STANDARD DEVIATION
6.59                  MINIMUNVALUE
9.05                  MAXIMUM VALUE
```

```
 9           ***
             ***
             ***      ***
             ************
 5           ***************                                      5
          ******************
    ************************
    ************************   ***                  ******
    *********************************      ***   ***************
 0  ------------------------------------------------------------  0
    +     +     +     +     +     +     +     +     +     +     +
  6.59  6.83  7.08  7.32  7.57  7.82  8.06  8.31  8.55  8.80  9.05
```

ISS DE-SELECTED AT 125C
IN UNITS OF MILLIAMPERES

FIGURE 7-17. DISTRIBUTION OF MEASURED ISS (DE-SELECTED) VALUES AT +125°C

```
55                    NUMBER OF MEASUREMENTS
8.37363636            MEAN
.7?7480671            ONE STANDARD DEVIATION
7.74                  MINIMUNVALUE
10.6                  MAXIMUM VALUE
```

```
                ***
                ***         ***
 5           ******         ***            ***                    5
       ***   *********      ***            ***
    ***************************            ***
    ***************************            ***   *********   ***
    ******************************   *********   ***************
 0  ------------------------------------------------------------  0
    +     +     +     +     +     +     +     +     +     +     +
  7.74  8.02  8.31  8.59  8.88  9.17  9.45  9.74  10.0  10.3  10.6
```

ISS SELECTED AT 125C
IN UNITS OF MILLIAMPERES

FIGURE 7-18. DISTRIBUTION OF MEASURED ISS (SELECTED) VALUES AT +125°C

55	NUMBER OF MEASUREMENTS
•397272728	MEAN
•0694773864	ONE STANDARD DEVIATION
•31	MINIMUNVALUE
•77	MAXIMUM VALUE

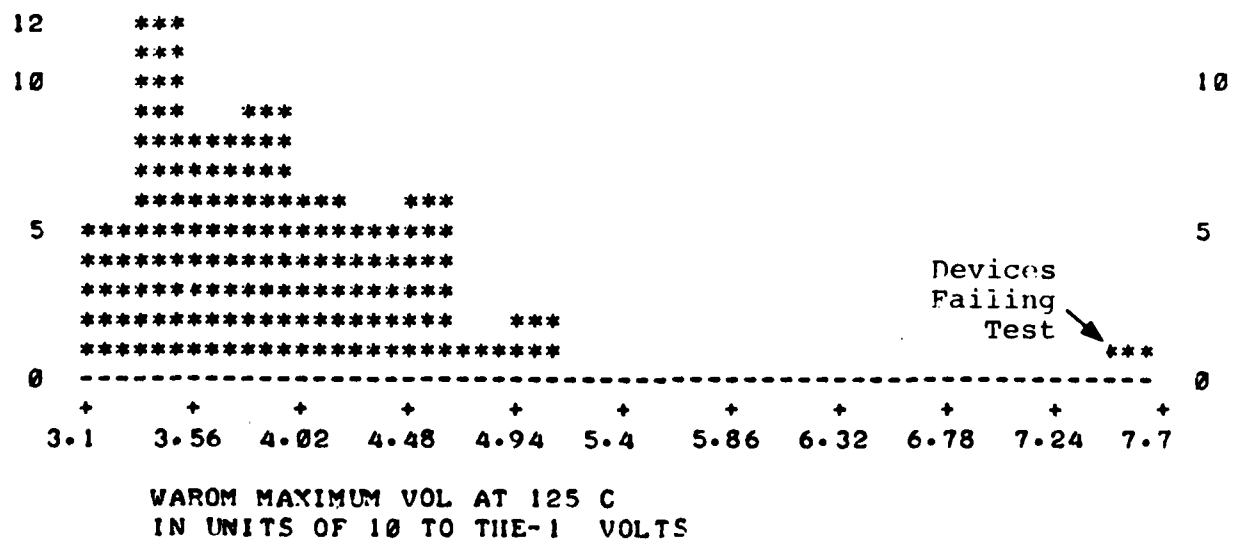


FIGURE 7-19. OUTPUT VOLTAGE LEVEL (VOL) AT SPECIFIED LOAD OF ER3400/NCR2451 AT +125°C

```
.M A651
A651, D5, D0
A652, 00,
.G 0

OK
GOTO170
 55                    NUMBER OF MEASUREMENTS
 4.10472728            MEAN
 .0337827628           ONE STANDARD DEVIATION
 4.03                  MINIMUNVALUE
 4.17                  MAXIMUM VALUE
```

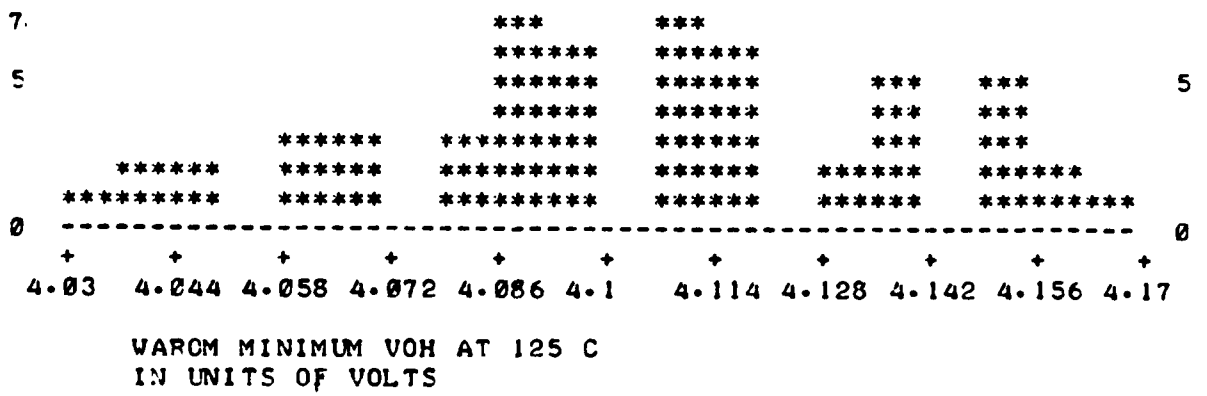
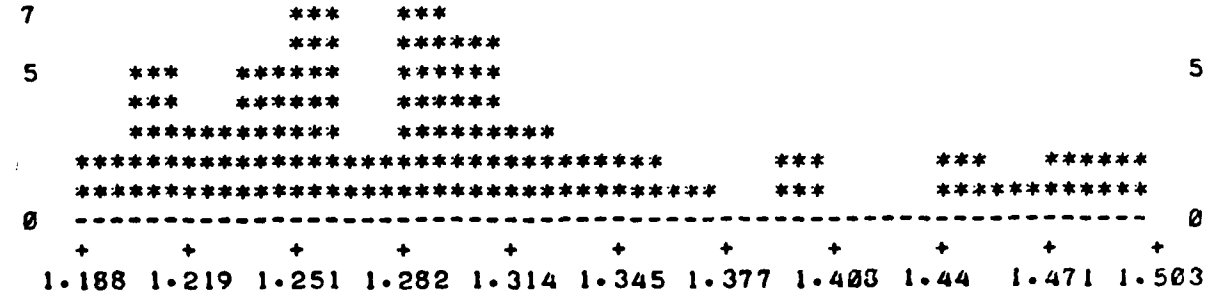


FIGURE 7-20. OUTPUT VOLTAGE LEVEL (VOH) DISTRIBUTION OF ER3400/NCR2451 PARTS TESTED AT +125°C UNDER SPECIFIED LOAD CONDITIONS

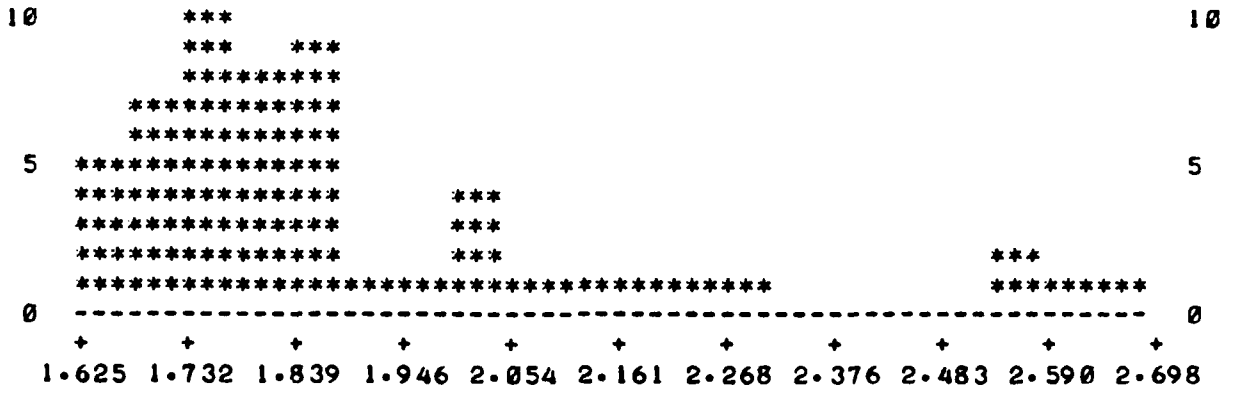
54	NUMBER OF MEASUREMENTS
13.0390741	MEAN
.812436398	ONE STANDARD DEVIATION
11.88	MINIMUNVALUE
15.03	MAXIMUM VALUE



WAROM IDD DESELECTED AT -55 C
IN UNITS OF 10 TO THE 1 MILLIAMPERES

FIGURE 7-21. IDD (VDD=-13V) DISTRIBUTION AT -55°C IN DE-SELECTED MODE FOR ER3400/NCR2451

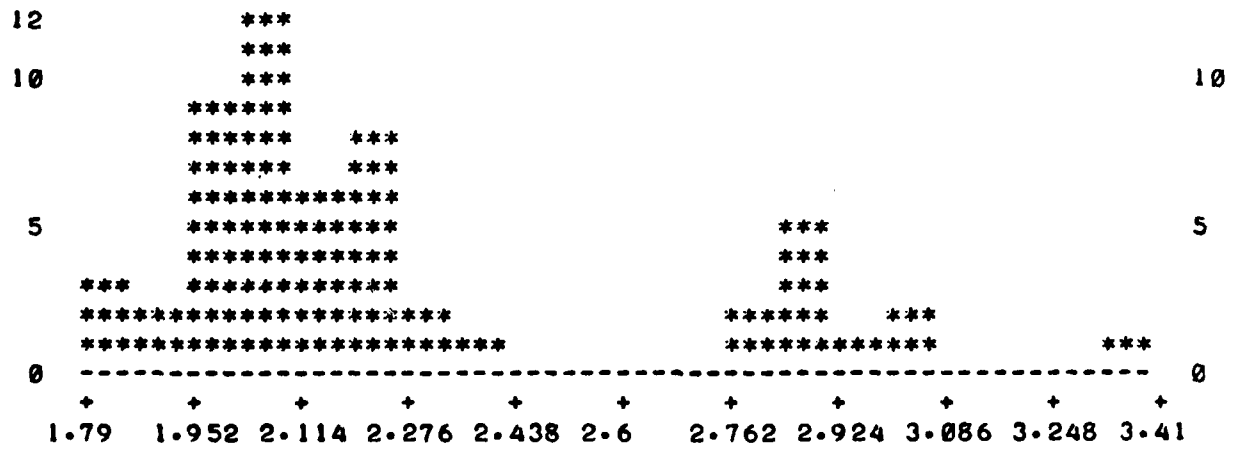
54	NUMBER OF MEASUREMENTS
18.96	MEAN
2.52249424	ONE STANDARD DEVIATION
16.25	MINIMUNVALUE
26.98	MAXIMUM VALUE



WAROM IDD SELECTED AT -55 C
IN UNITS OF 10 TO THE 1 MILLIAMPERES

FIGURE 7-22. IDD (VDD=-13V) DISTRIBUTION AT -55°C IN SELECTED MODE FOR ER3400/NCR2451

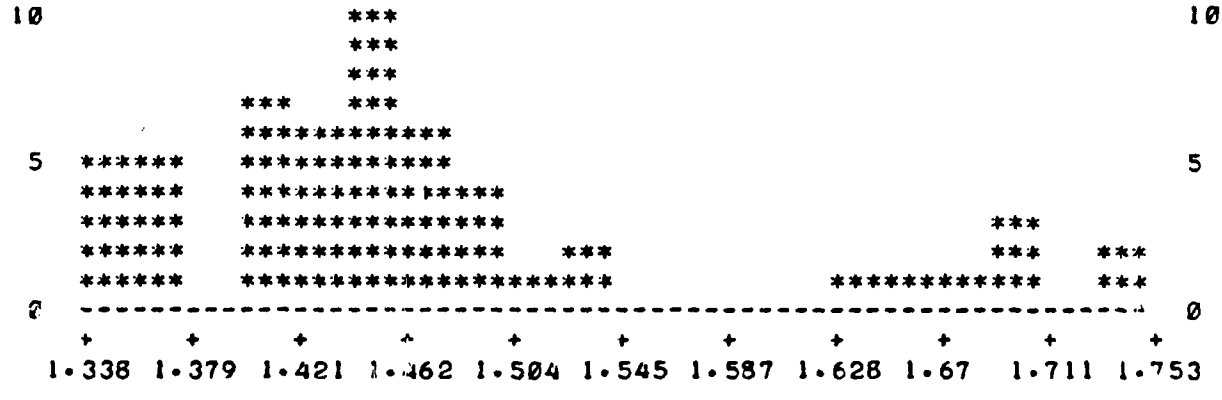
54	NUMBER OF MEASUREMENTS
2.26886889	MEAN
.371910315	ONE STANDARD DEVIATION
1.79	MINIMUNVALUE
3.41	MAXIMUM VALUE



WAROM IGG AT -55 C
IN UNITS OF MILLIAMPERES

FIGURE 7-23. IGG (VGG=-13V) DISTRIBUTION FOR ER3400/NCR2451 PARTS AT -55°C

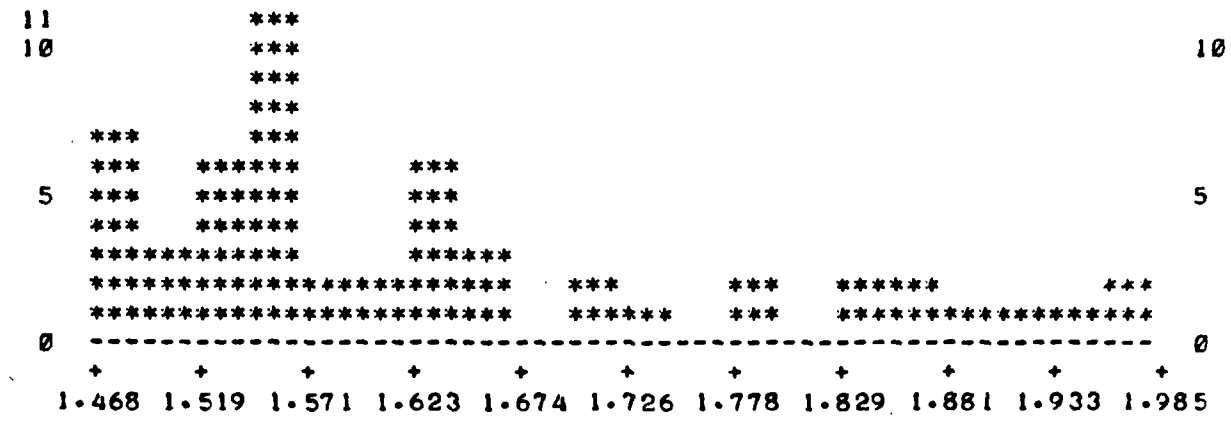
54	NUMBER OF MEASUREMENTS
14.7272222	MEAN
1.06926664	ONE STANDARD DEVIATION
13.38	MINIMUNVALUE
17.53	MAXIMUM VALUE



WAROM ISS DESELECTED AT -55 C
IN UNITS OF 10 TO THE 1 MILLIAMPERES

FIGURE 7-24. ISS (VSS=+5V) DISTRIBUTION AT -55°C FOR ER3400/ NCR2451 PARTS IN THE DE-SELECTED MODE

54	NUMBER OF MEASUREMENTS
16.3618519	MEAN
1.42944954	ONE STANDARD DEVIATION
14.68	MINIMUNVALUE
19.85	MAXIMUM VALUE



WAROM ISS SELECTED AT -55 C
IN UNITS OF 10 TO THE 1 MILLIAMPERES Iss in max 10^{-1}

FIGURE 7-25. ISS (VSS=+5V) DISTRIBUTION AT -58°C FOR ER3400/NCR2451 PARTS IN THE SELECTED MODE

Output voltage levels of ER3400/NCR2451 improve at -55 degree C as can be seen in Figures 7-26 and 7-27.

7.1.5 Final Functional Test. As is shown in Figure 7-1, the 55 parts remaining after DC parameter testing were reduced to 50 parts after final functional testing. The loss at this stage of the screening process was due to five NCR2451 parts that would not operate at -55 degree C in a normal READ, WRITE or ERASE mode. All of the devices that failed except one (1) would operate at -40 degree C. The conclusion drawn is that the oscillator circuit internal to the device was marginal in starting at this temperature.

7.1.6 Screened Parts Delivery To ERADCOM. Table 7-3 lists the serial numbers of parts passing the screen tests shown in the Test Plan. These parts were shipped to ERADCOM.

8. ACCELERATED TESTING OF TIME RELATED PARAMETERS IN MNOS MEMORIES

Testing of non-volatile memories with finite non-permanent periods of unpowered retention presents unique and difficult problems to test engineers. This complex problem is further complicated by the fact that the retention characteristic is dynamic in that it changes as a function of the device write/erase history. These factors add a third and fourth dimension to the normal two dimensioned memory test problem.

Since real-time measurement of retention characteristics is impractical; measurement of the change of that parameter as a function of device history is even less feasible. In the case of many MNOS type non-volatile memories the threshold of the memory array transistors can be measured and observed over a period of time. Since the threshold of the memory device is a direct function of the amount of charge trapped in the Nitride/oxide interface in the gate region it decays at the same rate as the discharge of the gate.

This fact allows the thresholds to be plotted as a logrithmic function of time depicting the retention characteristic of the device. by measuring and plotting several threshold points overtime, the line established by these points on a lin-log graph can be extrapolated out to the end of retention point and used to predict retention. Figure 8-1 shows this approach and points out how to find end of retention points for use in predicting retention.

```
54                  NUMBER OF MEASUREMENTS
4.39777778          MEAN
.0301641865         ONE STANDARD DEVIATION
4.32                MINIMUNVALUE
4.45                MAXIMUM VALUE
```

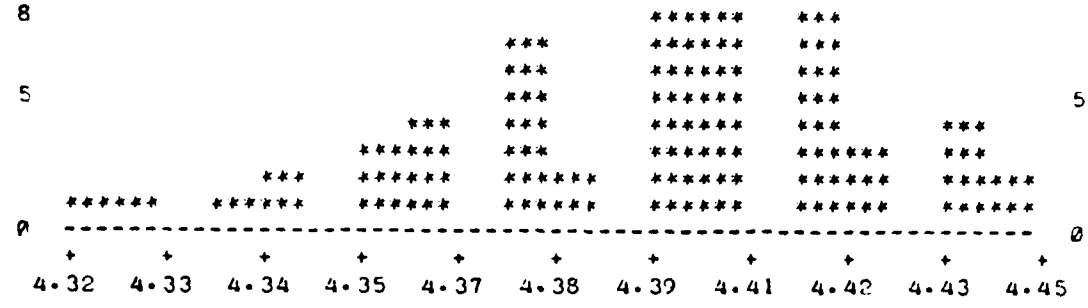


FIGURE 7-26. OUTPUT VOLTAGE LEVEL (VOH) AT -55°C FOR ER3400/NCR2451

```
54                  NUMBER OF MEASUREMENTS
.1S7222222          MEAN
.0352985499         ONE STANDARD DEVIATION
.13                 MINIMUNVALUE
.4                  MAXIMUM VALUE
```

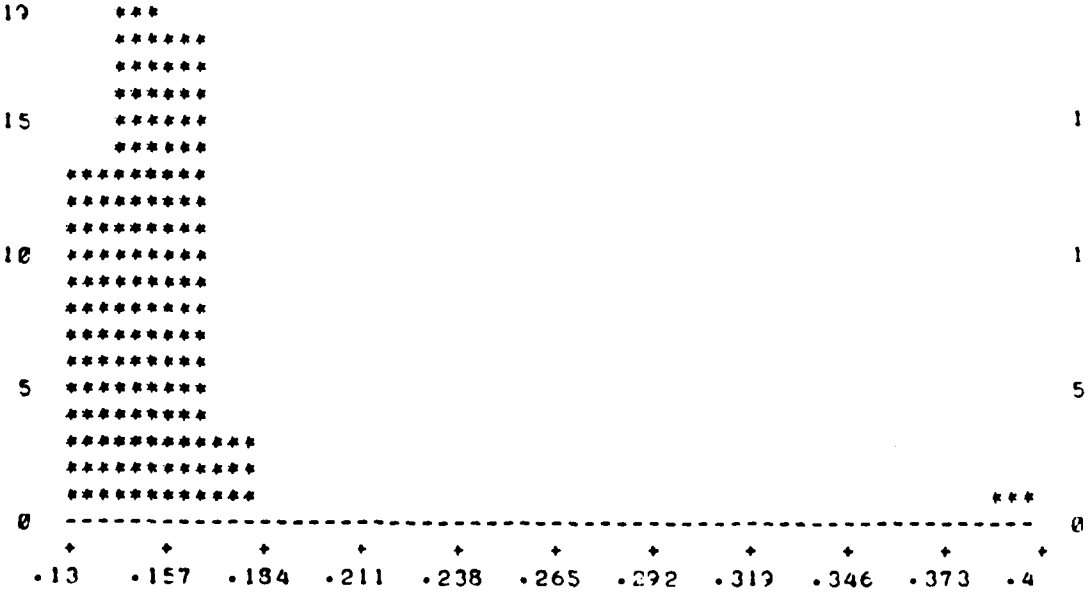


FIGURE 7-27. OUTPUT VOLTAGE LEVEL (VOL) AT -55°C FOR ER3400/NCR2451

TABLE 7-3. SERIAL NUMBERS OF PARTS PASSING FINAL SCREEN IN MACI PROGRAM

778	ER3400
782	ER3400
783	ER3400
8Ø3	ER3400
816	ER3400
822	ER3400
826	ER3400
829	ER3400
83Ø	ER3400
831	ER3400
832	ER3400
833	ER3400
835	ER3400
836	ER3400
84Ø	ER3400
841	ER3400
844	ER3400
845	ER3400
846	ER3400
849	ER3400
851	ER3400
852	ER3400
853	ER3400
854	ER3400
855	ER3400
858	ER3400
86Ø	ER3400
861	ER3400
864	ER3400
868	ER3400
869	ER3400
871	ER3400
872	ER3400
874	ER3400
875	ER3400
879	ER3400
88Ø	ER3400
884	ER3400
886	ER3400
887	ER3400
889	ER3400
89Ø	ER3400
2ØØ2	NCR2451
2ØØ6	NCR2451
2ØØ9	NCR2451
2Ø11	NCR2451
2Ø13	NCR2451
2Ø15	NCR2451
2Ø19	NCR2451
2Ø23	NCR2451

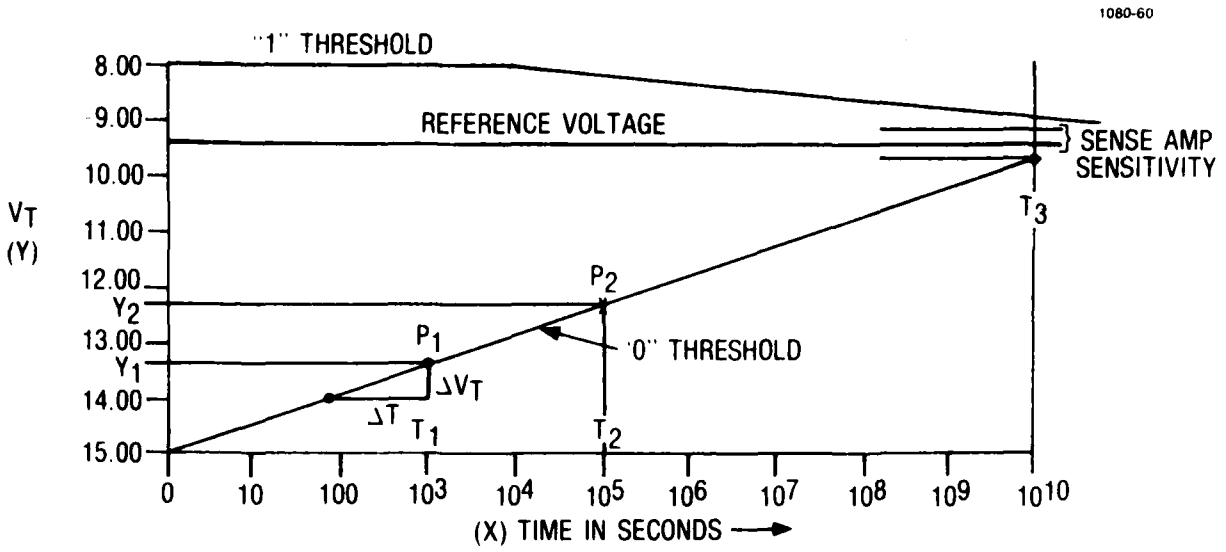


FIGURE 8-1. RETENTION PREDICTION CURVE

Using the diagram in Figure 8-1, an equation for the "0" threshold decay line can be written. Using the equation for a straight line:

$$y = mx + b$$

where y = device threshold @ end of retention

m = slope of retention curve $= \Delta Vt/\Delta T$

$$m = \frac{Y_2 - Y_1}{\text{Log}\left(\frac{T_2}{T_1}\right)}$$

x = retention time (logrithmic)

b = threshold at write time (i.e., $T = 0$)

$$= Y_2 - \text{Log } T_2\, m = Y_2 - \text{Log } T_2 \left(\frac{Y_2 - Y_1}{\text{Log}\left(\frac{T_2}{T_1}\right)}\right)$$

$$Y = \left[\frac{Y_2 - Y_1}{\text{Log}\left(\frac{T_2}{T_1}\right)}\right] (X) + Y_2 - \text{Log } T_2 \left(\frac{Y_2 - Y_1}{\text{Lg}\left(\frac{T_2}{T_1}\right)}\right) \quad (1)$$

Solving for x

$$x = \left(\frac{(Y - Y_2)\ \text{lg}\left(\frac{T_2}{T_1}\right)}{Y_2 - Y_1}\right) + \text{lg } T_2 \quad (2)$$

$$Tr = \log^{-1} x$$

Tr = actual retention time

y = the end of retention amplitude which for the case shown is the reference voltage minus the sense amp offset.

Since all points on the right side of equation (2) are known it can be solved producing the log of the retention time. By taking anti-log the predicted retention time can be found.

A more practical way to use this approach is to develop a minimum retention curve based on the specified device retention using an

initial threshold point and the end of retention point to establish the minimum retention curve. By taking a second threshold measurement, all that needs to be established is that when plotted on the curve that it falls below the line for the time point the measurement was taken. Equation (3) derived from equation (1) above shows this relationship.

$$y = \left[\log\left(\frac{T_2}{T_1}\right)\right]\left(\frac{V_{ref}-V_{off}-V_{T1}}{\log\left(\frac{T_{RET}}{T_1}\right)}\right) + V_{T1} \qquad (3)$$

where $y = V_T$ of second measurement

T_2 = time of second measurement

T_1 = time of first measurement

V_{REF} = internal reference voltage

V_{OFF} = sense amp offset voltage

VT_1 = threshold voltage of first measurement

T_{RET} = specified retention time.

Therefore the measured value of threshold at T_2 must be more negative than the value of y calculated above in order to have a retention characteristic greater than the specified retention.

The "one" threshold is not used for this calculation for several reasons. The normal tri-gate structure of the MNOS transistor causes the threshold plot to be stable for an undetermined length of time making short time measurements unfeasible. Furthermore due to the more significant read disturb effect and the shallower discharge slope of the one threshold, the "zero" threshold is designed to be the sooner of the two thresholds to decay by time related effects to intersect with the reference voltage and hence loss of ability to sense device state.

To further reduce the effort needed to predict device retention and minimize the test costs, a method was developed using separate bins for the initial threshold measurement instead of establishing the actual value. This is done because measuring the actual threshold is time consuming test wise and thus impractical as a screening test. By establishing a specified number of "bins" a

device threshold falls into, the number of measurements then equals the number of bins plus one. By "binning" the parts based on the initial threshold measurement, and using the nomograph (Figure 8-2,) which was developed from equation (3) test time is reduced significantly. Typical V_{T1} distributions shown in Figure 8-3a and b), were used to develop the nomograph.

The nomograph is used as follows:

RETENTION NOMOGRAPH USE

- Three hours after writing the device is binned according to VT1. VT1 need not be established to do this.
- Devices which operate with VGG = -30 and fail to operate with VGG = -11.54 are put in bin one.
- Devices which operate with VGG = -11.54 and fail to operate with VGG = -12.18 are put in bin two.
- Devices which operate with VGG = -12.18 and fail to operate with VGG = -12.82 are put in bin three.
- Devices which operate with VGG = -12.82 and fail to operate with VGG = -13.46 are put in bin four.
- Devices which operate with VGG = -13.46 and fail to operate with VGG = -14.10 are put in bin five.

After the 160 hour period the threshold voltage VT2 and the reference voltage are measured at room temperature. A line is established on the nomograph through VT1 on the left scale and the reference voltage on the center scale. The point where this line intersects the right scale is the minimum value which VT2 may be for the device to have a retention of one year. If the measured value of VT2 is greater (more negative) than this minimum; the projected data retention of the device is in excess of one year. Using the value of VT2 as the VGG value during read, a single measurement of whether the device reads correctly will determine if the retention is in excess of the one year requirement.

Figure 8-4 and the discussion below demonstrates use of the nomograph. On July 18, 1980 GI3400 #829 was written and soaked at 125°C for one hour. Three hours from the time of writing the threshold voltage VT1 was measured to be -13.54 volts. This is between -14.1 and -13.46 which is the only information required to use the nomograph.

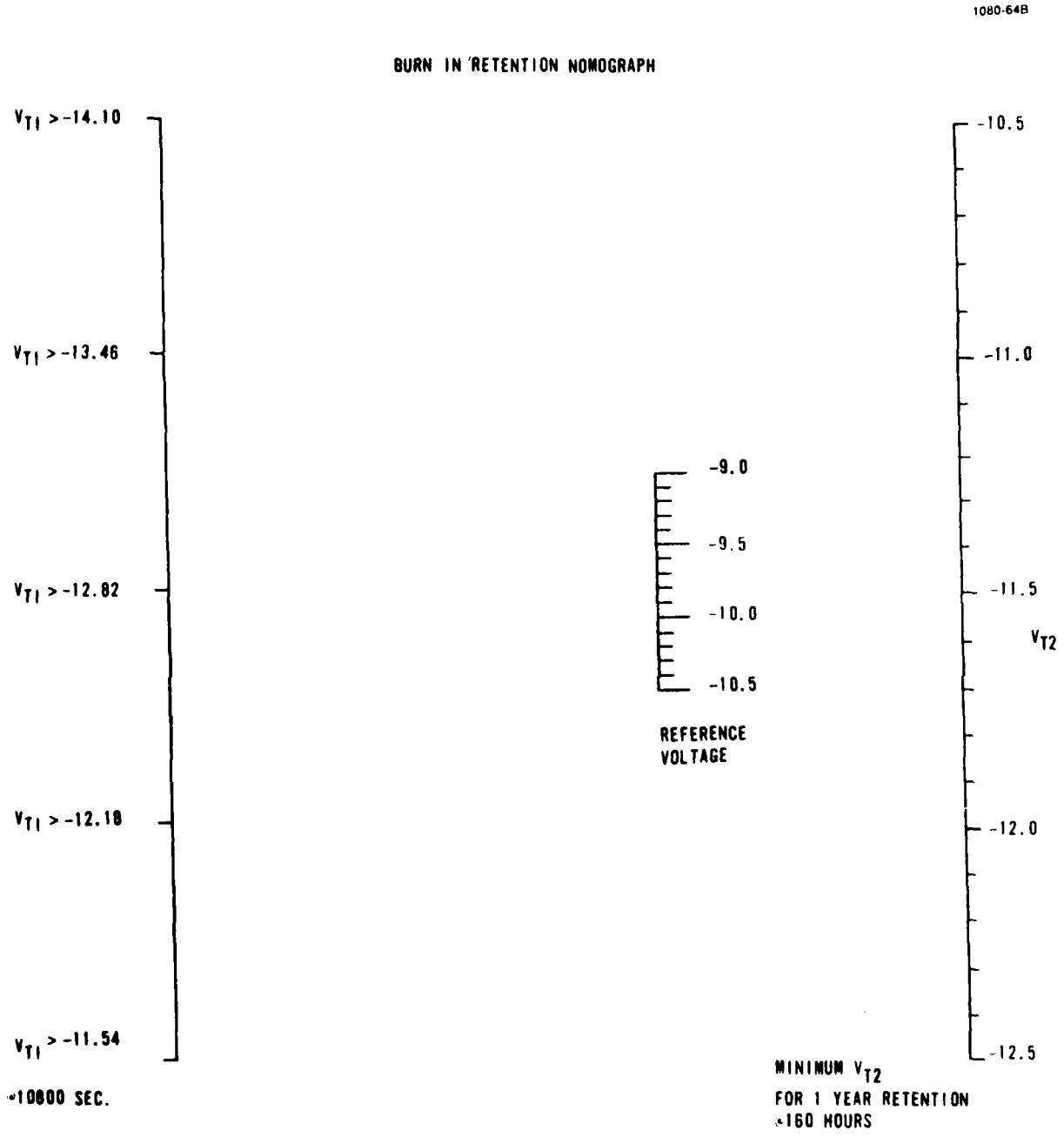


FIGURE 8-2. RETENTION NOMOGRAPH FOR ER3400/NCR2451 DEVICES

93	NUMBER OF MEASUREMENTS
-13.2739785	MEAN
.455910095	ONE STANDARD DEVIATION
-15	MINIMUNVALUE
-12.2	MAXIMUM VALUE

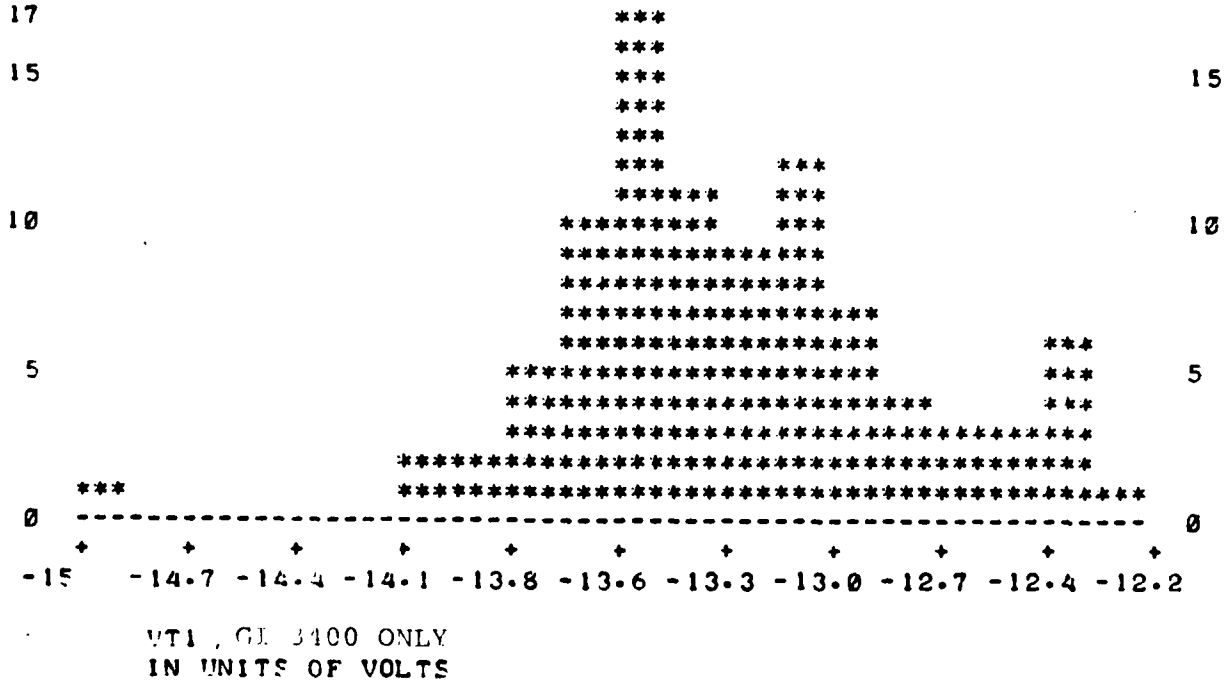
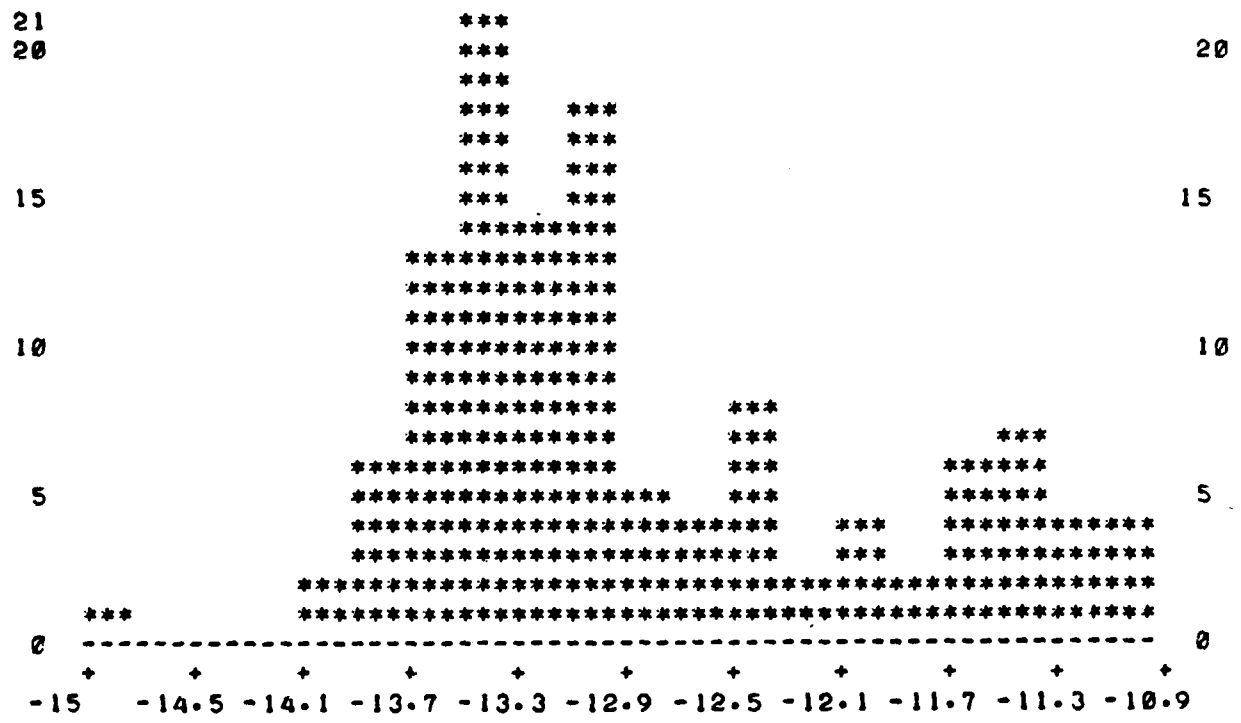


FIGURE 8-3a. VT1 OF SCREENED DEVICES

121	NUMBER OF MEASUREMENTS
-12.8753719	MEAN
.845710767	ONE STANDARD DEVIATION
-15	MINIMUNVALUE
-10.92	MAXIMUM VALUE



VT1 OF ALL TESTED MACI WAROMS
IN UNITS OF VOLTS

FIGURE 8-3b. VT1 OF ALL TESTED MACI WAROMS

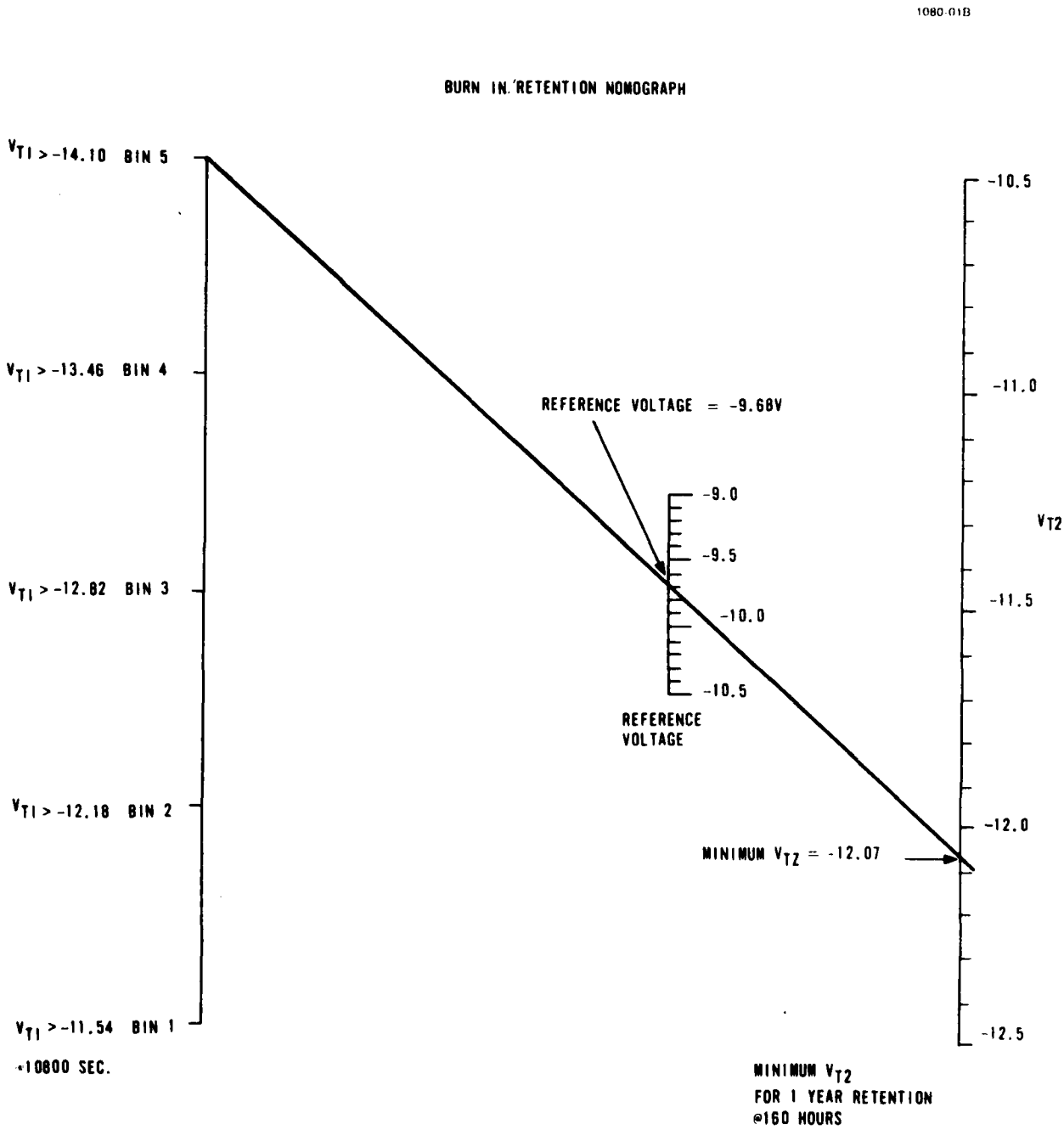


FIGURE 8-4. NOMOGRAPH USE EXAMPLE PROBLEM

The reference voltage of this device was measured to be -9.68 volts. A line is drawn on the nomograph through -14.1 on the left scale and -9.68 on the center scale. This line intercepts the right scale at minimum VT2 = -12.07 volts. After 160 hours at 125 degree C VT2 was measured to be -12.42 volts which is greater than the required minimum. Therefore device 829 has a predicted retention greater than a year at 125 degree C as required. The data is plotted on Figure 8-5.

This method of predicting retention characteristics significantly simplifies this task and allows devices to be screened in a practical way for this important parameter. Retention however, is not a fixed static condition but changes as a function of temperature and the number of write and erase cycles performed on a particular memory cell.

Temperature effects, while causing a reduction in retention from 10 years at +25 degree C to as low as 1 year at +125 degree C, can be measured and predicted using the normal techniques developed above. By using the prescribed 160 hour burn-in required by MIL-STD-883-B as a high temperature soak period for measuring retention, testing for this parameter fits conveniently into the normal screening schedule.

The change in retention as a function of the number of erase/write cycles performed on a particular cell (known as endurance) is a much more complex testing matter. Since the effect is a permanent change, unlike retention, normal tests on a screening basis for real time measurement of endurance are impractical. Due to endurance being measured as a function of retention, and with retention being a long expensive test, screening for this parameter is furthur complicated. Methods currently in use apply lot sampling methods to eliminate low endurance parts from systems. The correlation between sampled devices and the lot is tenuous at best. This allows poor endurance parts to be placed in field use or eliminates the use of these cost effective memories due to low confidence levels of screening out bad parts.

It was noticed by NCR that devices having thinner nitride layers than others in any batch of similar devices exhibited lower endurance levels when used in systems where nominal voltages were set to optimize the performance of the full range of devices. Using this fact, Honeywell, in cooperation with NCR and GI, developed some functional, user oriented, tests that measures relative nitride thickness of the memory devices. Correlation tests were performed to determine if the thinner nitride devices exhibited poorer endurance. The results were positive and these tests were developed to be used at screening levels to provide a much lower risk method of eliminating poor endurance parts. Since the data base is yet fairly small, direct prediction of endurance is not yet practical but relative endurance between devices is now feasible.

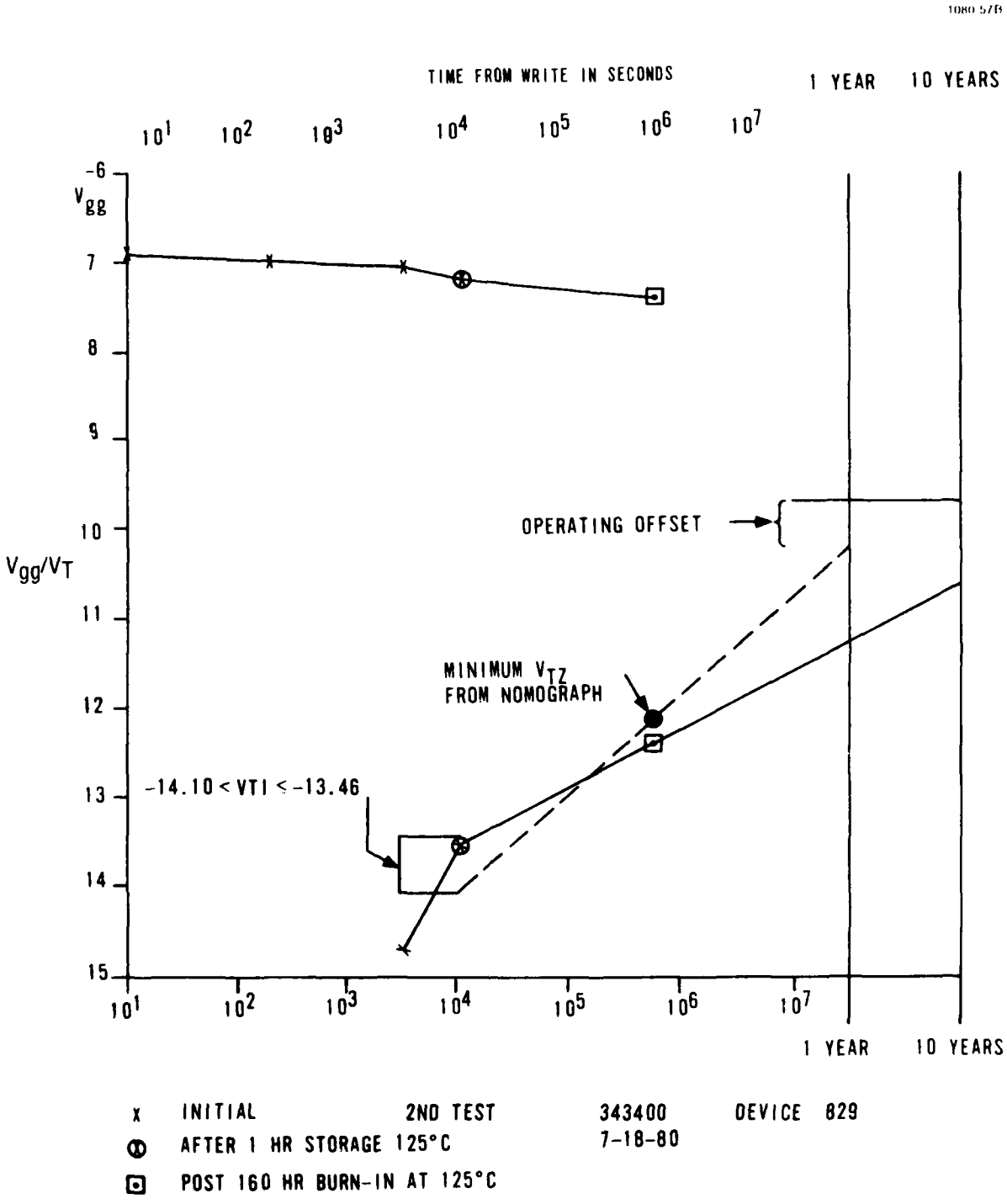


FIGURE 8-5. PLOTTING OF SAMPLE PROBLEM DATA

Since it was known that thicker nitrides results in slower erasing devices, a qualitative soft erase method was developed to indicate relative nitride thickness. A normal write cycle was used, followed by an erase cycle reduced in both applied bias and width. The threshold was measured after this cycle, and devices that showed the greatest change in threshold from the written state were sorted out to be thin nitride parts thus having lower endurance characteristics than other parts. Since some parts do not have threshold measuring capability, a method using a series of short erase cycles, each followed by a read cycle, show which devices change state first, indicating thinner nitride parts. Much of the data linking these conditions were shown in the earlier MACI report (Interim #1).

Figure 8-6 shows the retention of particular MNOS devices after 10^5 erase/write cycles plotted against the soft erase threshold measurement being proposed to predict that performance. It can be clearly seen that devices having a lower (less negative - greater change) soft-erase threshold exhibit a poorer retention after 10^5 E/W cycles. While the curves shown are for all types tested, it can be seen that the 2401 show the worst correlation. This was probably due to unstable threshold measurement characteristics exhibited by the devices.

Using a best fit curve technique, Figure 8-7 plots the measured soft erase thresholds against the post 10^5 E/W cycle retention and produces a curve from which to extrapolate endurance predictions. Table 8-1 shows the basis for the curve and the correlation of the curve to the measurements. Some of the values of screened devices were placed on the curve showing predicted retentions after 10^5 E/W cycles of 7.4×10^4 seconds and 3.3×10^5 seconds.

Using a data base of 225 parts the distribution of soft erase thresholds measured is shown in Figure 8-8. Using Figure 8-7 to predict endurance, the range of retention after 10^5 E/W cycles indicated by this distribution is from 3×10^4 to 5×10^6 seconds. Table 8-2 lists the prospective endurance values for all NCR2451's passing the screen tests.

It should be understood that the data base for the threshold measurement to endurance correlation is still very thin and should be characterized over a wider range of lots. Further correlation between memory substrate leakage current on devices where this output is available (i.e., NCR2810/ER2810) and soft erase thresholds points toward using dc leakage measurements to sort out low endurance parts. The results of that investigation are shown below.

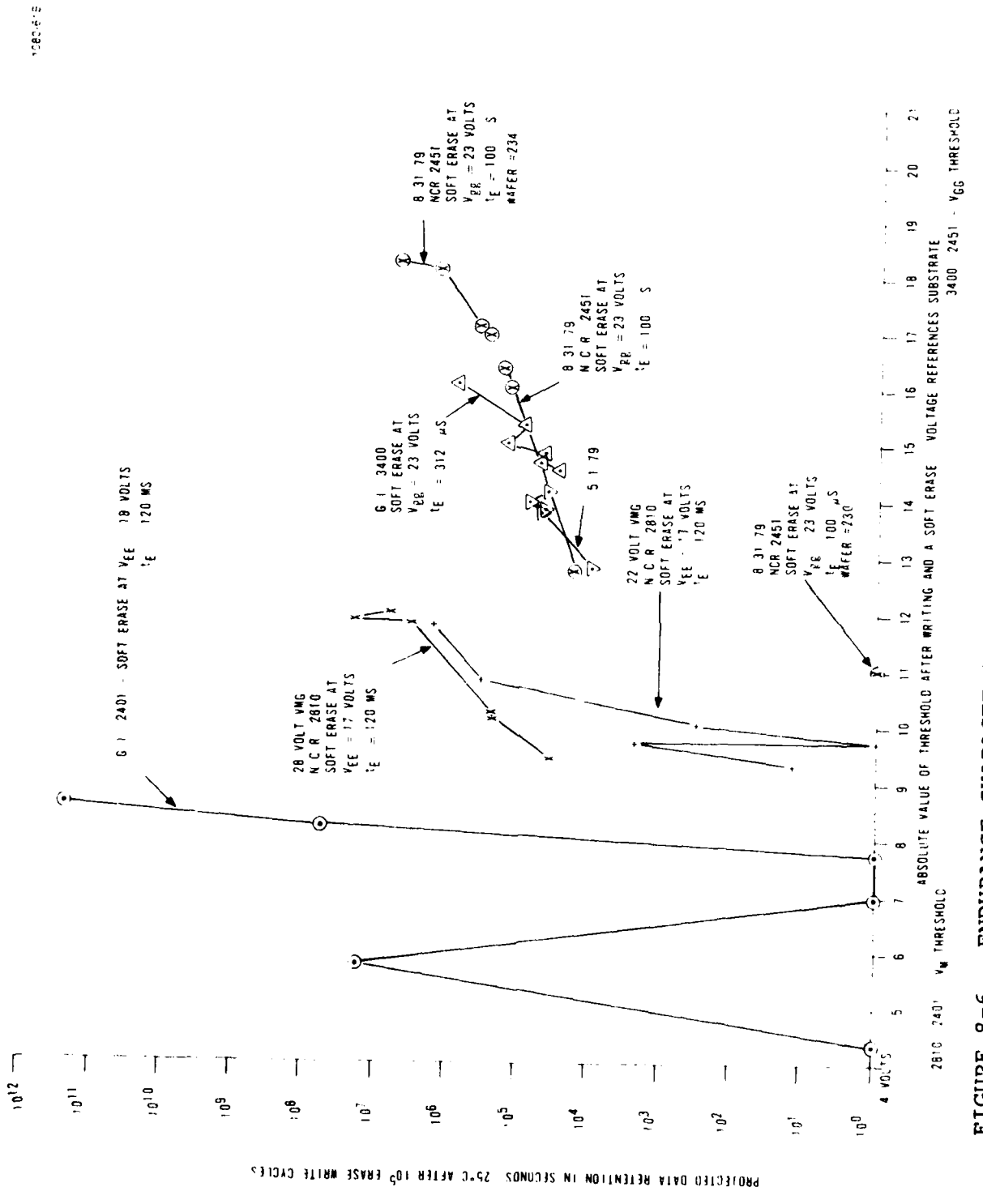


FIGURE 8-6. ENDURANCE CHARACTERISTICS FOR MNOS DEVICES AS A FUNCTION OF SOFT ERASE THRESHOLD MEASUREMENT

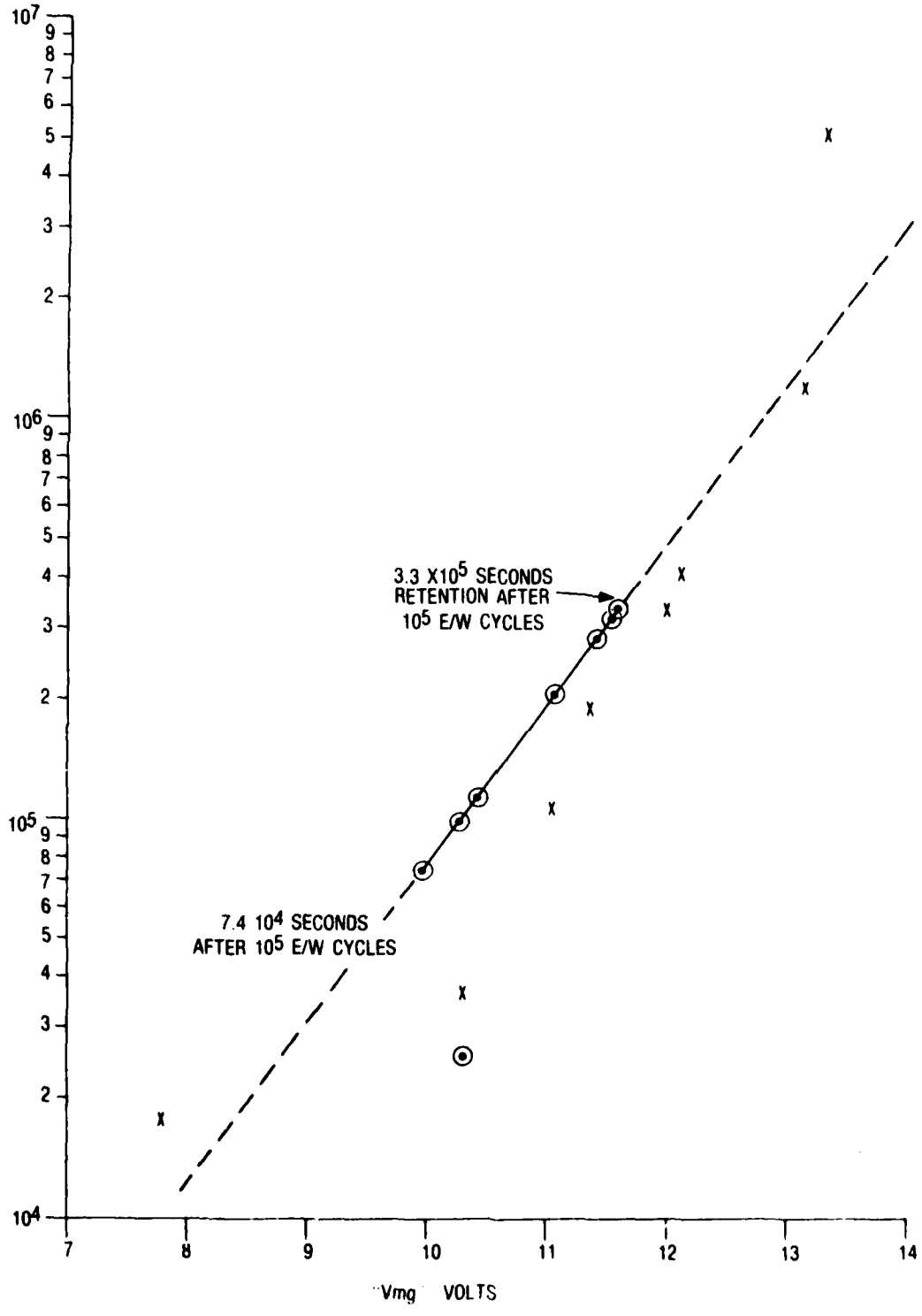
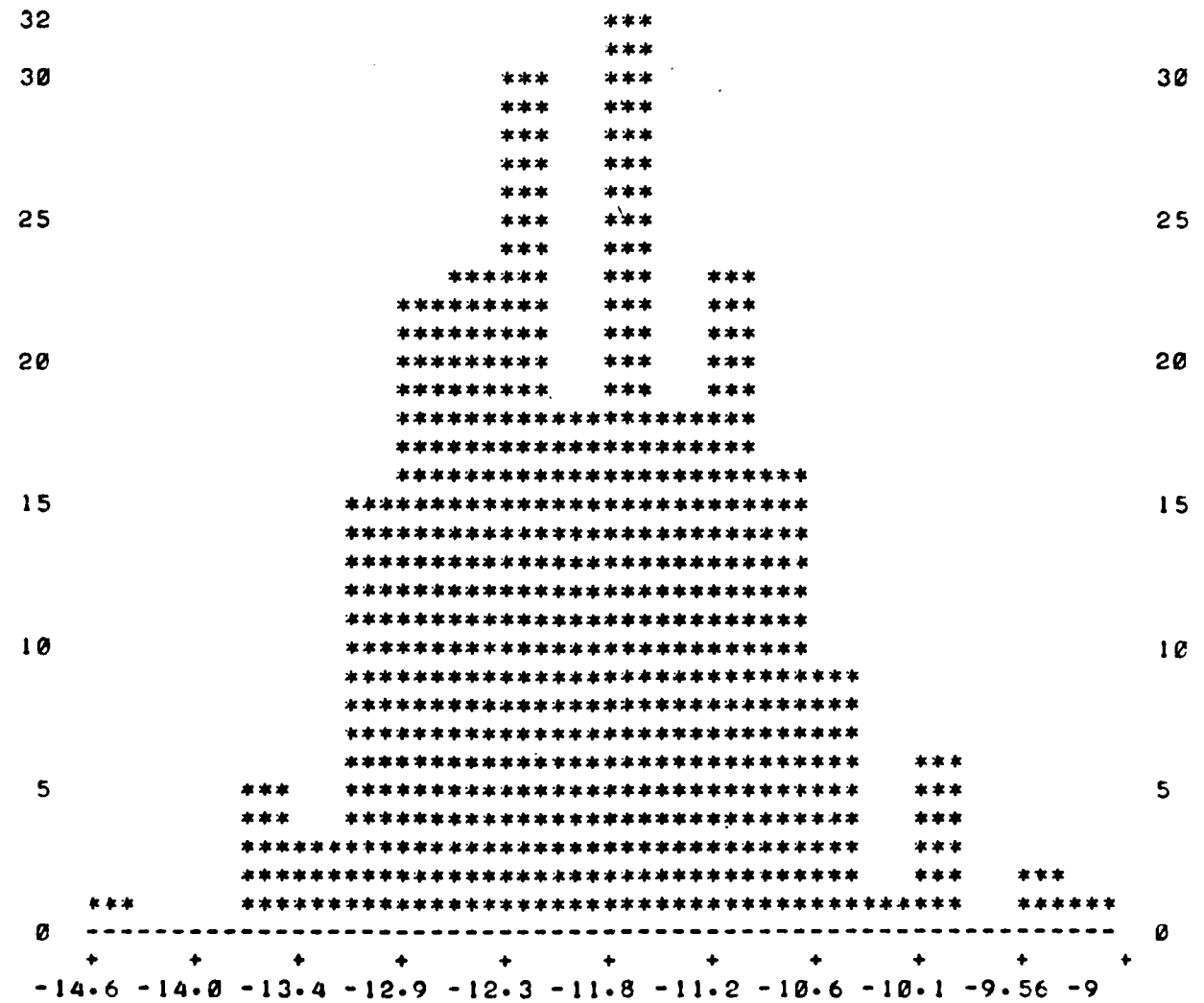


FIGURE 8-7. ENDURANCE VERSUS SOFT ERASE THRESHOLD

225	NUMBER OF MEASUREMENTS
-11.8704	MEAN
.886579477	ONE STANDARD DEVIATION
-14.62	MINIMUNVALUE
-9	MAXIMUM VALUE



ZERO THRESHOLD OF ALL TESTED MACI WAROM MEMORIES
IN UNITS OF VOLTS AFTER WRITING ZEROS AND A SOFT ERASE

FIGURE 8-8. SOFT ERASE THRESHOLD DISTRIBUTION FOR PREDICING ENDURANCE

TABLE 8-1. 2451 ENDURANCE

Device	"VMG"	Retention @1ØØØØØ EW	Log of Retention
535	-12.ØØ	337ØØØ	5.528
537	-13.3Ø	516ØØØØ	6.713
539	-13.12	12ØØØØØ	6.Ø79
546	-12.1Ø	416ØØØ	5.619
512	-7.8Ø	178ØØ	4.25Ø
515	-11.Ø4	1Ø8ØØØ	5.Ø33
527	-11.36	192ØØØ	5.283

Least square linear fit of log of retention to "VMG" Log of retention=Ø.934-Ø.396"VMG" Correlation coefficient=-Ø.936 retention=8.59ØEXP-(Ø.912"VMG")

TABLE 8-2. ER3400 ENDURANCE

Device	VMG	Projected Retention in Seconds After 10^5 EW
2ØØ2	-11.Ø6	2Ø6347.874
2ØØ6	-11.54	31968Ø.946
2ØØ9	-11.58	331558.232
2Ø11	-11.42	286541.521
2Ø13	-9.94	743ØØ.9291
2Ø15	-1Ø.26	9948Ø.6798
2Ø23	-1Ø.42	1151Ø9.454

This paper is a brief summary of comparisons of erase substrate leakage current (IEEL) to: (1) read threshold after soft erase (VT) and (2) number of soft erase (#SE) until an indeterminate zero threshold level is reached.

Read threshold after soft erase and the number of soft erases until an indeterminate zero threshold level is reached has been demonstrated to be related to each other and to gate nitride thickness and therefore, endurance. These comparisons were performed to determine if a reasonable correlation could be observed between IEEL and VT/#SE. A more detailed explanation of endurance and VT tests is included in the MACI preselection report.

DEFINITIONS

Erase Substrate Leakage Current (IEEL) - In a block erase type EAROM only, the leakage current from substrate to gate during the erase cycle.

Soft Erase - Erasing a device using either reduced erase voltage or reduced time (from recommended specification).

Read Threshold After Soft Erase - The device "0" (minimum) threshold (VT) after a normal write and a soft erase.

For other definitions, see MACI preselection report.

The results of the data comparison are shown for the 2810 device type in Table 8-3 and similarly for the 2401 device type in Table 8-4. The devices are listed in increasing IEEL order.

Figure 8-9 represents a plot of the log of IEEL versus VT for the 2810 device type. The trend of increasing IEEL with decreasing VT is apparent.

Although the data base was small, a direct relationship between IEEL and VT (and thus endurance) has been demonstrated. This simple static test can easily be incorporated into the standard DC screening tests. This test, in addition to VT and other tests, could increase the confidence of users in eliminating inferior endurance parts. With additional characterization, a direct correlation between IEEL and number of erase/write cycles until nitride fatigue occurs may be obtained. A maximum IEEL limit may be imposed, depending on reliability requirements, for each device type. This limit could be specified according to the number of erase/write cycles anticipated for the useful life of the devices.

TABLE 8-3. DEVICE: 2810

Serial Number	IEEL(A)	Number of Soft Erases	Read Threshold After Soft Erase (Volts)
302	-2	285	No Data
333	-3	275	-6.79
320	-6	125	-6.73
325	-8	33	-6.24
336	-12	20	-5.99
323	-16	22	-5.81
328	-18	24	-5.88
322	-22	7	-5.54
316	-29	1	-5.42
339	-47	6	-5.51
319	-61	4	-5.06
317	-80	1	-5.43
344	-82	6	-5.21
331	-91	2	-4.84
326	-96	2	-4.71
321	-125	3	-5.07
318	-170	2	-4.98
332	-276	2	-4.8
327	>-1500	1	-4.72

TABLE 8-4. DEVICE: 2401

Serial Number	IEEL(A)	Number of Soft Erases	Read Threshold After Soft Erase (Volts)
410	-1	1200	-4.78
428	-1	264	-4.7
417	-3	73	-3.66
409	-4	10	-2.52
401	-22	5	-2.04
407	>-1500	1	-.92
423	>-1500	1	No Data

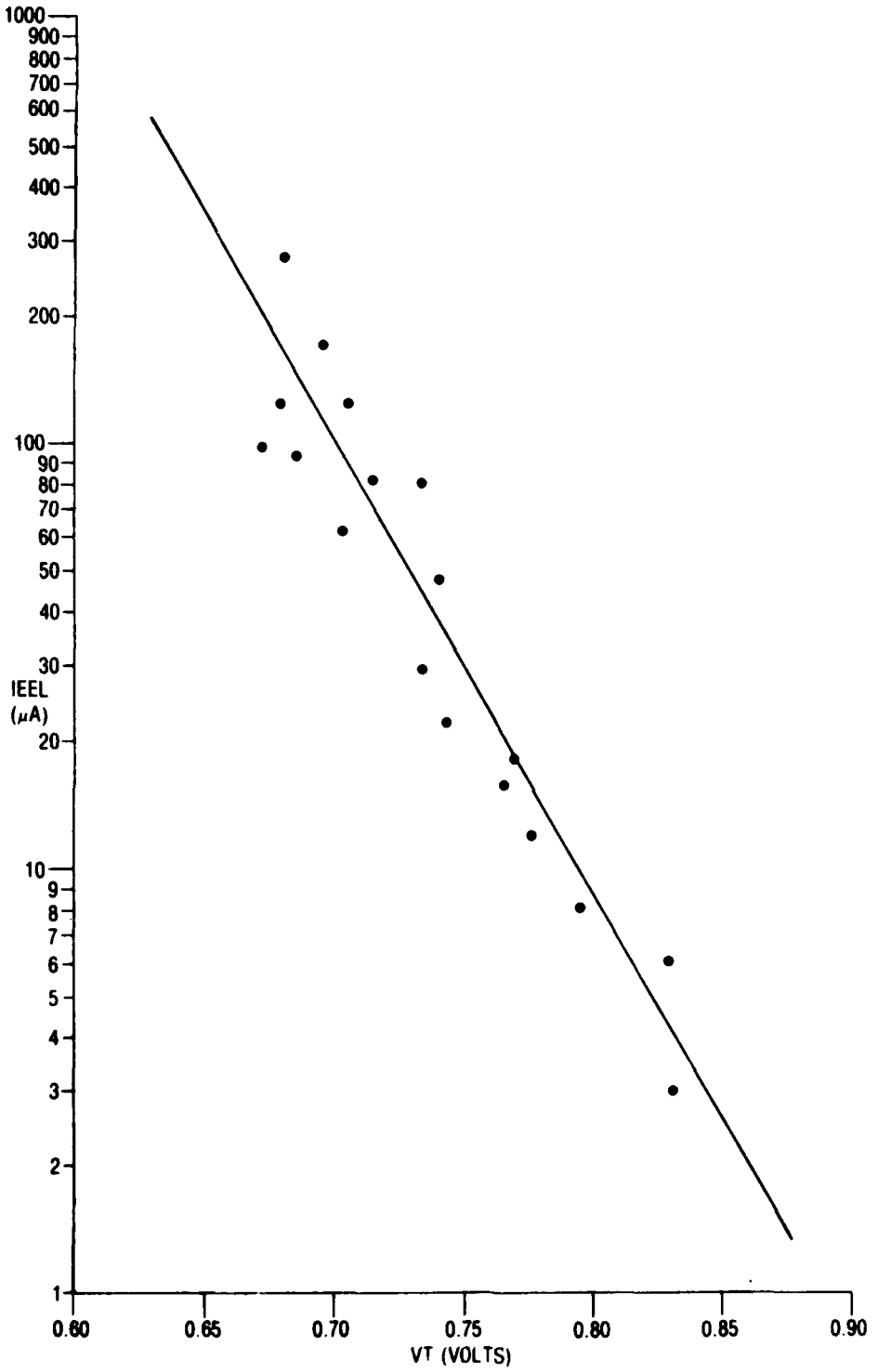


FIGURE 8-9. ERASE SUBSTRATE LEAKAGE CURRENT (IEEL) VERSUS READ THRESHOLD (VT)

The use of any of the measurements to indicate endurance, assuming the correlation to real endurance is as tight as the early data base indicates, significantly reduces the risk of poor endurance parts finding their way into systems and improves the confidence level of potential users to bring MNOS devices into a broader range of applications.

An investigation into the relationship between the speed of writing characteristics and the read disturb effect in MNOS memories was started. Results of that investigation, while promising in the trends it shows, have produced no conclusive results thus far. Due to the tremendous time expenditure and tieing up of equipment, results require extended periods to compile and analyze and dedicated programs to finance. If these tests prove fruitful, the last time related parameter will be able to be predicted in a practical way.

9. CONCLUSIONS

After completion of the Third Phase of the MACI EAROM Program the following conclusions can be drawn:

- The MACI Program has attempted to define and organize the testing and evaluation of MNOS Memory Devices at a time when little formal definition of those methods exists.
- The Accelerated Tests developed under this program will significantly contribute to the reliability of the screen tests and reduce the expense of testing EAROMs.
- Unique test patterns (i.e., assymetric slant) developed under MACI enable test engineers to test for worst case patterns while performing address integrity tests simultaneously.
- Characterization of devices by users should be a continuous program in order to insure that small process changes do not affect parameters critical to the operation of the devices in systems.
- Due to the time related parameters of MNOS, things affecting device performance sometimes take long periods of time before being noticed and corrected.
- A new generation of non-volatile memories is being developed which will require the same careful evaluation as the previous parts before a high confidence level can be obtained for their use in systems.
- The proposed Final Slash Sheet will contain the latest approaches to measuring EAROM viability that have been developed and reflect the status of the MNOS industry.